End of Master Degree Project

Master in Energy Engineering

Analysis and simulation of a MMCC-SSBC converter

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Abstract

Battery energy storage systems (BESS) are the most versatile type of energy storage. With an increasing share of renewable energy, they could prove to be essential to provide the much needed flexibility. The MMCC-SSBC might be the most suitable converter for modern BESS. It is modular, and allows for an individualized treatment of the connected battery modules. The main objective of this thesis is to develop a tool which simulates the behavior of a MMCC-SSBC converter. This objective is fulfilled by the core deliverable of the thesis: a Matlab implementation of a dynamic model of the converter. As a secondary objective, this thesis aims to demonstrate the usefulness of this tool. It applies the tool to a specific use case, and analyzes three key characteristics based on the simulations: efficiency, power quality and reliability. This leads to some concise design guidelines, and continued operation under a battery short-circuit fault.

Contents

Chapter 1

Introduction

1.1 Context and motivation

Nowadays, climate change and it's human cause is an established scientific fact. In the words of the intergovernmental panel on climate change:

> The SYR confirms that human influence on the climate system is clear and growing, with impacts observed across all continents and oceans. Many of the observed changes since the 1950s are unprecedented over decades to millennia. The IPCC is now 95 percent certain that humans are the main cause of current global warming. [1]

Emissions of greenhouse gases have reached an unprecedented height [1]. This led to several international initiatives to tackle greenhouse gas emissions. In 2007, the European Union (EU) agreed on a climate and energy package, setting specific targets for 2020. The three key targets are a 20% cut in greenhouse gas emissions, a 20% of EU energy from renewables and a 20% improvement in energy efficiency. [2]. By enacting this package, the EU strives to fight climate change, create green jobs and secure energy supplies. Additionally, the EU launched the Horizon 2020 programme. It is the biggest EU Research and Innovation programme, containing €80 billion of funding. With this, the EU seeks to drive economic growth and create jobs. [3]

More flexibility is essential to accommodate renewable generation in the energy mix. Flexibility is not new; flexible generators already allow the system to balance the supply and demand [4]. Traditionally, flexibility is provided by the supply side [5]. But recently, more and more renewables entered the energy mix. The EU for example committed to increasing the share of renewables to 20% by 2020 [2]. Variable

renewable energy sources (RES) cannot provide supply side flexibility due to their lack of controllability [5]. On the contrary, they heighten the need for flexibility due to their volatility. Signs of an inflexible power system include difficulty balancing supply and demand, renewable energy curtailments, price volatility and negative market prices [4]. One promising source of flexibility is energy storage.

Generic energy storage could provide several services. They can be classified in two broad categories according to duration. Short-duration services include frequency control and system stability services, whilst long-duration services include energy management and power reserves. Which functions are more prominent for a given storage type, depend on its key characteristics: response time, capacity both in terms of power and energy etc. Battery energy storage systems (BESS) are the most versatile type of energy storage. They can do peak shaving, defer investments in transmission and distribution, regulate voltage, replace spinning reserve and many more [6, 7]. A common value proposition is using BESS in conjunction with a renewable energy source. For example, Prompinit and Khomfoi use a BESS to reduce the volatility of PV generation in a microgrid [8].

Battery modules and a power converter are the main components of a BESS. The power converter forms the interface between the battery modules and the electrical grid. Traditional BESS use a multipulse converter together with a complicated zigzag transformer [9]. This transformer has several disadvantages: it is expensive, bulky and likely to fail [10]. Instead, modern BESS use a multilevel converter. Maharjan et al. developed a BESS which uses a MMCC-SSBC converter [10]. They further claim that the MMCC family of topologies might be the most suitables ones for modern BESS. These topologies are modular, and allow for individualized treatment of the connected battery modules. These are desirable characteristics.

1.2 Objectives and scope

The main objective of this thesis is to develop a tool which simulates a MMCC-SSBC converter. Such a tool is crucial for the design and analysis of a BESS based on this type of converter. Therefore, as a secondary objective, this thesis attempts to demonstrate the potential of this tool. Based on simulations carried out by the tool, the thesis will analyze key characteristics of the converter and provide design recommendations.

A functional converter is a complex device, with several levels of control. For each of these levels of control, there are multiple methods available in the literature. Therefore,

the scope for each of these individual levels is narrow. This thesis chooses the most conventional and straightforward control methods rather than the very latest experimental ones. Specifically, rotating frame PI-control and sub-harmonic unipolar PWM are implemented. The merit of this thesis will not be to advance one of those levels of control, but to bring all those levels together in one simulation tool. Furthermore, this thesis considers only the converter itself. It models the grid as an infinite bus and the batteries as ideal voltage sources.

1.3 Outline

This thesis contains 7 chapters and several appendices. The current chapter, the introduction, starts of by showing the reader the motivation for this research. It continues with defining the research objective and the scope of it. Finally, this section clarifies the structure of the document.

The upcoming chapters follow roughly the flow of the actual research. First, chapter 2 reviews the literature and identifies the state-of-art, relevant to the construction of the simulation tool. It covers a wide range of literature. Next, Chapter 3 clarifies the methodology. It shows in detail all the steps of the research, and how they are connected.

Chapter 4 and 5 contain the core of the work. Based on the literature, chapter 4 develops in-depth a model of the SSBC-MMCC converter. Chapter 5 describes the developed tool and applies it to a case study. The analysis discusses three key characteristics: efficiency, power quality and reliability.

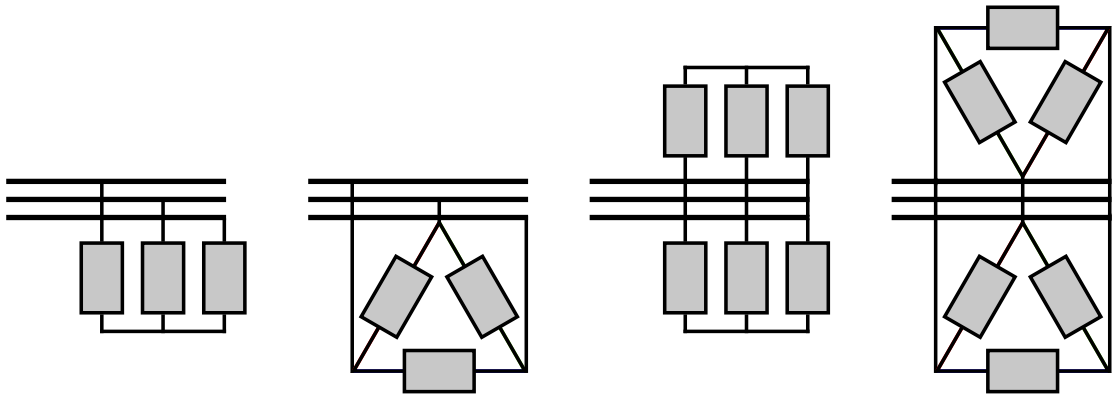
Finally, chapter 6 concludes the thesis with a summary of the obtained results and suggestions for further research. Chapter 7 expresses the gratitude of the author of this thesis towards the people who enabled this work.

Chapter 2

Literature review

In the past, researchers have proposed several names for the MMCC-SSBC converter. These names reflect some of the key characteristics. Akagi studied the history of the converter, and proposed a naming convention and classification based upon it [11]. The converter is both modular and cascaded. The converter wires together several H-bridge or chopper cells, which are the building blocks of the converter. Cells are connected in series to create the multilevel output [12]. Hence, the converter consists of groups of cascaded modules, hereafter referred to as clusters. This justifies the first half of the name: modular multilevel cascade converter (MMCC). Two things remain undefined: the topology and cell type. Firstly, Fig. 2.1 shows four variations of the topology. Secondly, the cell type is uniform across the converter, and is either a chopper cell (CC) or an H-bridge cell (BC). This leads to the second half of the name: single star bridge cell (SSBC).

Ota et al. recommend the MMCC-SSBC converter for use in a BESS. It provides a cost-effective, practical and flexible solution [13]. Maharjan et al. researched this setup extensively, validating the results with an experimental verification [10, 14–16]. These studies provide a high-level discussion, assuming a background knowledge on several topics such as current control, pulse width modulation (PWM) techniques and many more. Knowledge on all of these topics is required to build a fully functional simulation tool. Therefore, the remainder of this chapter will discuss the state-of-art regarding several of these topics.



(a) SS (b) SD (c) DS (d) DD

Figure 2.1: The topology is characterized by two letters. The first letter is either S or D, which stands for single and double. This refers to the number of clusters per phase. The second letter is also either S or D, but stands for star and delta instead. This refers to how the clusters are interconnected.

2.1 Current control

Bahrani et al. discuss the methods which have been developed for current control [17]. Over the years, several controllers emerged. They can be classified in two main groups: linear and non-linear controllers. The non-linear techniques add additional complexity, but without a significant improvement in performance. Therefore, linear controllers are the most popular. A further distinction is based on the used reference frame. The linear controllers can be applied either directly or after transforming the signals to the rotating frame. Bahrani et al. state that the most well-known control method is a PI-controller applied in the rotating frame [17]. Schauder et al. proposed this method more than two decades ago [18]. This method is easy to implement and provides a satisfactory performance.

This thesis will adopt the conventional rotating frame PI-controller. Bahrani et al. recognize its satisfactory performance, but also mention some disadvantages [17]. In the rotating frame, the current has two components, direct and quadrature. The conventional approach decouples these two components and applies a separate PI-controller to each component, ignoring the cross-coupling. In a real system however, some cross-coupling remains. The decoupling is based on the system parameters, so deviations in these parameters affect the cross-coupling. Furthermore, disturbances in one component also affect the other control loop.

For these reasons, Bahrani et al. propose two modified controllers to tackle these

issues [17, 19]. In a first study, they propose a multivariable PI-controller [17]. This controller offers better axis decoupling, and is less sensitive to system parameter uncertainty. In a second study, they propose a non-parametric controller. By experimental verification, they conclude that this controller has the best dynamic performance. Implementing these controllers is beyond the scope of this thesis. It is significantly more complex, whilst the conventional approach already offers a satisfactory performance.

2.2 Modulation

The modulation technique enables the synthesis of the voltage waveform. It affects the charging and discharging of the energy storage elements, the harmonic distortion and associated switching losses [20]. The switches are the controllable elements of the modules. In multicarrier PWM methods, the switching signals are generated by comparing a reference signal to a carrier.

Konstantinou et al. give an oversight of multicarrier PWM techniques [20]. There are two main methods: the carrier-disposition method and the sub-harmonic method. The carrier-disposition method divides the voltage range in bands. When the target voltage moves within a certain band, only the corresponding module is active and changes its output. All modules below are turned on, and all modules above are turned off. There are three variants: PD, POD and APOD. They differ in the phase-shift applied to the carriers. The sub-harmonic method ,also known as PSPWM, activates all modules. When the target voltage rises, all modules scale their output and contribute to the voltage increase. The carriers are phase-shifted by equal distances, covering 360°. Because all modules are switching to realize the waveform, the effective switching frequency is elevated. Agelidis et al. [21] compared these techniques in terms of harmonic performance, and the impact of the number of modules. The harmonics caused by the carrier-disposition are locked around the carrier frequency, irregardless of the number of modules. The center of the harmonics caused by the sub-harmonic method shifts to higher frequencies when the number of modules increases.

In the modern design of a MMCC converter, each module has an isolated energy storage element. This requires additional modulation control. Besides synthesizing the voltage waveform, the modulation technique has to balance the energy level of the modules. There are two types of storage elements: capacitor banks and battery modules. The energy level of a capacitor bank strongly affects the output voltage. Therefore, the voltage waveform synthesis and energy balancing are linked. Table 2.1

Table 2.1: Several PWM techniques are able to balance the voltage of the capacitor banks in a multilevel inverter.

Abbreviation	Method	Source
PSPWM	phase-shift PWM	[21]
HPWM	hybrid PWM	[21]
CRPWM	carrier rotation PWM	[23]
MCRPM	modified carrier rotation PWM	[24]

shows several modulation methods which achieve voltage balancing of the capacitor banks. Hagiwara et al. describe in detail how PSPWM can achieve the voltage balancing [22]. When battery modules are used instead, the voltage balancing becomes less crucial. Battery modules have a relatively flat voltage profile [15]. Instead, a BESS has to be able to control the state-of-charge (SoC), a measure for the stored energy, of each battery module.

This thesis implements the PSPWM modulation technique. It provides a good harmonic performance and is straightforward to implement. Maharjan et al. describe on a high-level how this method can balance the SoC [15]. Under PSPWM, all modules are active and the SoC is achieved using continuous control signals alone. A carrier-disposition method on the other hand, has to swap the bands of the modules to balance the SoC. This would require a discrete logic. This thesis does not implement the SoC balancing, but chooses the PSPWM method to facilitate further research along these lines.

2.3 Reliability

Maharjan et al. reviewed several studies on 'fault-tolerance' in cascaded converters [16]. They divide the proposed techniques in two main categories, depending on whether redundant cells are added or not

1. A redundant converter cell is added to each phase. When a fault occurs in a cell, not only that cell is bypassed, but also one cell in the other two phases.

2. No converter cells are added. When a fault occurs, only the faulty cell is bypassed.

The first category has the advantage that it can continue to operate at rated power and voltage when a fault occurs. But this advantage comes at a cost: a redundant cell is added to the converter. The second category is exactly the opposite. It doesn't add

the cost of a redundant cell, but it can only operate below rated power and voltage when a fault occurs. It depends on the application whether this loss of available power is acceptable or not. [16]

The fault-tolerant operation technique depends on the modulation strategy. For example, Wei et al. developed a technique using the redundant switching states of the converter, with space vector modulation (SVM) [25]. Since this thesis chose for the combination of U-PWM and the sub-harmonic method instead of SVM, this technique is not applicable. Rodriquez et al. on the other hand developed a technique for a converter with a similar modulation strategy [26]. When a cell becomes faulty, the control system bypasses the cell. To compensate for this loss, the control system adjusts the phase shift of the trigger and the reference voltage of the remaining cells. Lezana et al. use a similar approach [27]. Ma et al. propose a reconfiguration method for both the carrier-disposition method and the sub-harmonic method [28].

2.4 Loss modeling

The switches are the main cause for the losses in a converter. An insulated-gate bipolar transistor (IGBT) fulfills the role of the switch. Additionally, freewheeling diodes are added across each IGBT in order to conduct the load current during the blanking period. These semiconductor components cause 4 types of losses: conduction losses, turn-on losses, turn-off losses and off-state blocking losses [29]. The duration of the switch transition is in the order of a few hundred nanoseconds [29]. The time step of the solver is typically larger than this. This makes it challenging to simulate the switching losses. There are two options: using a dynamic model or an algebraic model.

A dynamic model includes the waveforms of the switching transition in the simulation. The literature contains several models, with varying levels of modeling accuracy. There is a trade-off between accuracy and required computer resources to run the simulation. Which model is best, depends on the application and the required level of detail. Tominaga et al. use a physics based model for the static behaviour and voltage dependent capactitances to model the dynamic behaviour. The physics based model is solved numerically with a finite difference method [30]. Instead, Lauritzen et al. [31] and Schumann et al. [32] use an analytic physics based model. Schumann et al. provide a comparison with the results of a finite element model [32]. Overall, these dynamic models require a very small time step and a complex parameter extraction.

Rajapakse et al. propose an algebraic alternative to the dynamic model [29]. The

switching transition only lasts a few hundred nanoseconds, and therefore typically falls in between two steps of the solver. Rajapakse et al. developed parametric fits of the switch transition waveforms. These fits take into account the coupled physical effects of the IGBT and the diode. Based on these parametric fits, Rajapakse et al. derive equations for all switching loss components. The equations require two types of input: device-specific parameters and state variables. The data sheets provide the device-specific parameters. The state variables on the other hand depend on the current and voltage before and after the switch transition.

Kouro et al. analyze the losses of a MMCC converter with an algebraic model of the switching losses [33]. An algorithm superimposes the switching losses on the low-resolution dynamic simulation. Whenever the algorithm detects a switching transition, it calculates the switching losses based on the state variables at that time. The conduction lossed are directly included in the electrical circuit. A constant voltage drop in series with a linear resistance approximate the transfer characteristic well. This event-based model requires significantly less computer resources than a high-resolution dynamic simulation. However, the algebraic model used by Kouro et al. and Rajapakse et al. is still quite complex in terms of required parameters.

An empirical algebraic model simply fits measurements of the switching losses to model the current dependency. Dieckerhoff et al. propose such an empirical model [34]. The component data sheets typically provide a graph of the switching losses as a function of the current I, for a fixed voltage V_{ref}. Dieckerhoff et al. apply a quadratic fit to this graph. Furthermore, they include the voltage dependency by assuming it scales linearly compared to the reference voltage V_{ref}

$$E_{sw} = \frac{V}{V_{ref}} \left(a \cdot I^2 + b \cdot I + c \right)$$

ABB, a major IGBT producer, suggests the same approach [35]. Feix et al. expand this approach by including a model for the temperature dependency. Furthermore, they provide an alternative way to model the reverse recovery losses based on the reverse recovery charge and the current slope [36]. This model is useful when the manufacturer does not provide a graph of the current dependency. Finally, Cavalcanti et al. [37] and Alamri et al. [38] use a different approach to model the conduction losses; they use a quadratic fit instead. Alamri et al. argues that this is a better approach, because it is based on the actual transfer characteristic [38].

This thesis adopts a modified version of the event-based model of Kouro et al. [33].

The algebraic model is replaced by the one suggested by Dieckerhoff et al. [34] and ABB [35]. To counter the critique of Alamri et al. [38], the voltage drop and linear resistance are derived directly from the transfer characteristic. More complicated models tend to have a complex parameter extraction, which partially cancels the gained accuracy when only data sheets are available. The combination of the event-based approach of Kouro et al. [33] and the empirical model of Alamri et al. [38] offers a good computational performance, and a straight-forward parameter extraction.

Chapter 3

Methodology

The main objective of this thesis is to develop a tool for designing and analyzing a SSBC-MMCC converter. As a secondary objective, the thesis strives to demonstrate the usefulness of this tool. This is done by discussing three aspects of the converter: efficiency, power quality and reliability. This chapter will discuss the main steps taken in order to achieve these two objectives.

The research differs in structure from this document. This document presents the work as a sequential list of steps. In reality, the research had a more iterative nature, with exchanges and iterations between the steps. Fig. 3.1 shows a flow chart of the procedure followed by the research. There are 4 main steps: literature review, model development, Simulink implementation and use case analysis. These correspond roughly to three chapters in this thesis: literature review, modeling and control, and case study. Case study includes both the Simulink implementation and the case study. The remainder of this chapter will describe each of these steps in detail.

The literature review aims to identify the state-of-art concerning the SSBC-MMCC converter. The review goes from general to specific; high-level studies are followed by more specific ones, detailing specific parts of the state-of-art. First, more general literature regarding multilevel converters is reviewed. This sets the scene and provides the necessary context for the SSBC converter. Next, the review focuses on the SSBC, and how it can be used with batteries as energy storage elements. The composition of the topology, its basic operation principle and main characteristics are discussed on a high level by the literature. It assumes the reader has a working knowledge of power converters. Therefore, the review further focuses on specific topics necessary for the implementation of the converter. These topics are essential for the development of the specifics of the model.

The full model covers many topics in the literature. In order to reduce the complexity, this thesis separates the model in three interacting layers. These three layers are: interface and control, converter operation and loss model. Each layer is developed on its own. Within a given layer, the operation of the layer below is idealized with a set of assumptions. The layer itself is designed in order to achieve as closely as possible the assumptions of the layer above. By doing so, the model can temporarily ignore the underlying complexity and focus on the complexity in a specific layer. This layered approach facilitates significantly the Simulink implementation.

The Simulink implementation is interwoven with the model development. The layered structure of the model transfers to the Simulink implementation. First, the model of the top layer is developed and directly implemented in Simulink. Directly implementing the model deepens the understanding of it and points out potential shortcomings. If the underlying layer is needed in order to test the implementation, it can be replaced with a simplified version. For example, when implementing the interface and control layer, the converter was replaced by a controllable voltage source. This approach facilitates the debugging of the implementation, as the complexity of each implementation round is significantly reduced. This approach is repeated for each subsequent layer.

A base case offers a starting point for the simulation. Most of the parameters depend on the application. These parameters include the rated power, battery module voltage and cascade number. Furthermore, short circuit requirements are provided by the operator of the grid to which the converter is connected. All these are set to typical values, common for converters used in power grids. The main parameters to be sized, are the specifics of the filter. In the base case, the short circuit requirements lead to a minimal sizing of the filter. The effect on the harmonics is neglected in the base case. With all parameters set to specific values, the tool simulates the operation of the converter.

Running the simulation leads to a set of raw output data. In order to draw conclusions, several Matlab scripts convert the raw data to a more presentable form. Most importantly, the scripts convert the waveforms to the frequency domain, exposing the harmonic components. The base case does not consider the power quality of the output waveform in the initial sizing of the filter. Therefore, it is crucial to verify whether the harmonics stay within reasonable limits. Conceptually, the impact of the filter on the harmonics is assessed. Based on reasoning, the necessary sizing of the filter is predicted. Fig. 3.1 indicates this check with the purple box. If the power quality is

unacceptable, the chart flows back to the sizing step. This is iterated until the power quality falls within the required limits.

The steps described by Fig. 3.1 will fulfill the objectives of this thesis. The first three steps, literature review, model development and Simulink implementation, lead to a tool with and underlying model, based on relevant literature. The fourth step, case study, shows the usefulness of this tool. The case study uses the tool to size the filter in order to keep the harmonics within acceptable limits.

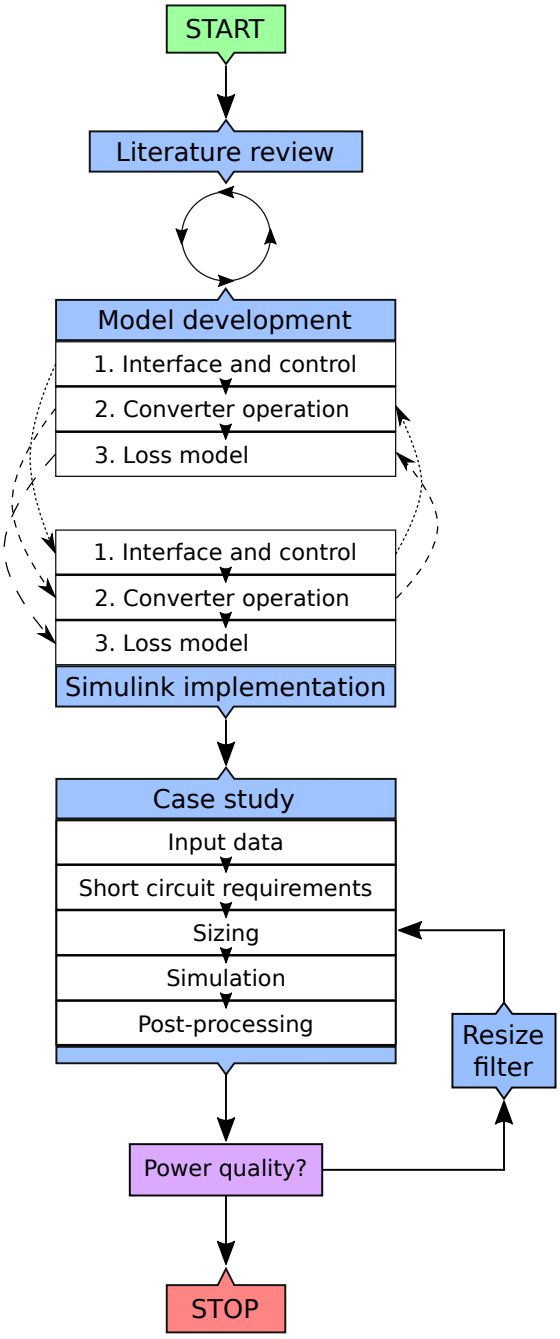


Figure 3.1: The thesis goes through 4 steps in order to achieve the objectives. The arrows indicate the interaction and flow between the steps.

Chapter 4

Modeling and control

With only three cascade levels, the SSBC-MMCC converter already contains 9 batteries, 36 IGBTs and 36 diodes. Proper grouping and simplification of sub-modules is necessary to properly understand the converter. This thesis divides the model in three layers. Each layer uses an idealized representation of the layer below and strives to approximate the assumptions made by the level above. Fig. 4.1 shows a schematic overview of the layers and their interaction. Some topics, such as harmonics reduction, are related to several layers. But for the purpose of conceptual understanding, this subdivision is useful.

For example, the top layer, interface and control, assumes the converter can instantly achieve an arbitrary voltage at its output. Based on this assumption, the top layer then implements a control loop which achieves the desired power output. The control loop generates a reference voltage for the converter, which is passed on to the middle layer (converter operation). The middle layer operates the converter in such a way that it approximately achieves the reference voltage.

This chapter is structured according to these three layers. Each of the following sections discusses a layer in detail, and mentions how it fits in the bigger picture. The order is top-to-bottom, in order to keep the reader engaged. The layer above states the purpose for the layer below through the assumptions it makes about it.

4.1 Interface and control

The top layer of the model regulates the power flow to the grid. It assumes that the converter can be represented by an ideal voltage source. Taking into account the parameters of the filter, the top layer implements a negative feedback control loop. The

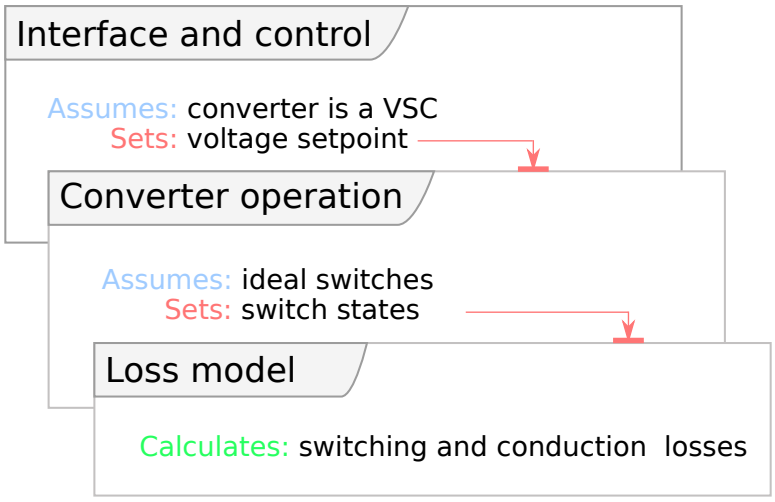


Figure 4.1: The thesis divides the model in three layers: interface and control, converter operation and real switches. Each layer assumes ideal operation of the layer below, and set the operation point for it.

control system adjusts the voltage of the VSC to obtain a specified power output. The power output is measured, and fed back through a control loop to adjust the voltage setting.

Fig. 4.2 shows a diagram of the top layer system. This section is organized in two subsections. The first subsection will derive the dynamic equations governing the electrical circuit. These equations are transformed to a more convenient form thereafter. The second subsection discusses the design of a control system to achieve the desired power output.

4.1.1 Electrical equations governing the system

Fig. 4.3 shows the electrical diagram of the system. Applying Kirchhoff's voltage law and the transfer characteristics of an inductor and a resistor, this leads to the set of equations shown by (4.1).

$$\begin{bmatrix} v_{Cu} \\ v_{Cv} \\ v_{Cw} \end{bmatrix} - \begin{bmatrix} v_{Su} \\ v_{Sv} \\ v_{Sw} \end{bmatrix} = L\frac{d}{dt}\begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + R\begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} \tag{4.1}$$

Alternative method for reverse recovery losses if not given directly in the datasheet, but in terms of reverse recovery charge and current slope

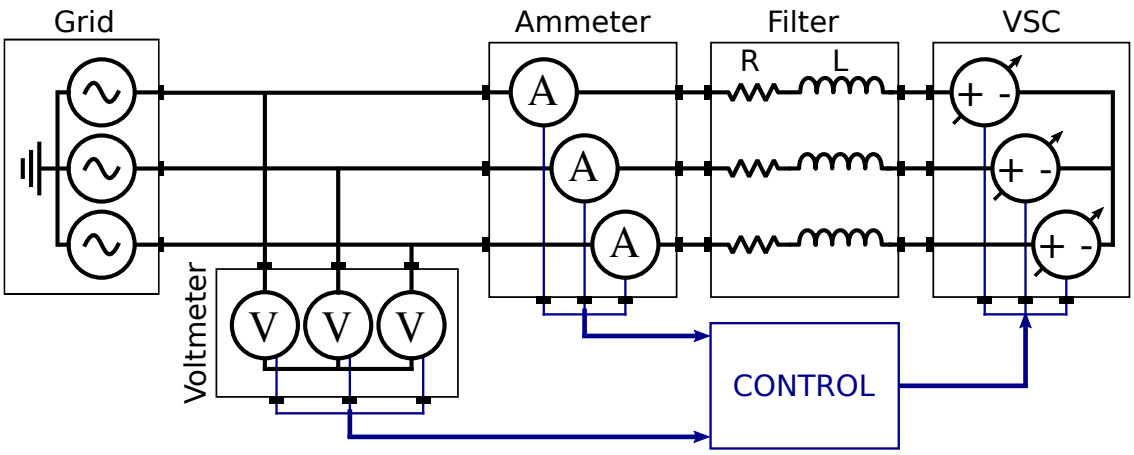


Figure 4.2: The control system measures both the voltage and current at the point of common coupling, at the grid tie. By doing so, the control system calculates the immediate power flow to the grid and sets the VSC accordingly.

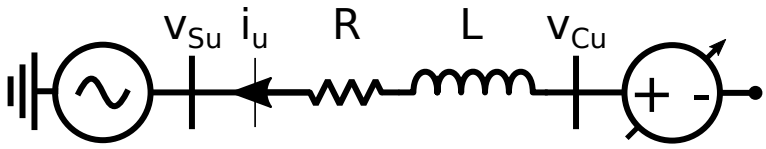


Figure 4.3: This diagram shows the electrical variables of the u-phase of the complete system displayed by Fig. 4.2. The other phases have an identical layout, the variable names are only changed according to the phase.

Fig. 4.2 shows clearly that there are two nodes in the system: the neutral point of the grid and the neutral point of the VSC. Applying Kirchoff's current law gives only one linearly independent equation, shown by (4.2). The sum of all phase currents is equal to zero, since there is no return wire.

$$i_u + i_v + i_w = 0 \tag{4.2}$$

Equations (4.1) and (4.2) can be combined in an elegant way by transforming equation (4.1) to the dq0 reference frame. The full derivation is left for Appendix D. The set of equations (4.3) show the final result of the transformation.

$$\begin{bmatrix} v_{Cd} - v_{Sd} \\ v_{Cq} - v_{Sq} \\ v_{C0} - v_{S0} \end{bmatrix} = \left(L \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} + R \right) \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \tag{4.3}$$

$$\Rightarrow \begin{bmatrix} v_{Cd} - v_{Sd} \\ v_{Cq} - v_{Sq} \end{bmatrix} = \left(L \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \end{bmatrix} + R \right) \begin{bmatrix} i_d \\ i_q \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{4.4}$$

Since the sum of the phase currents is equal to zero, this implies that the 0-component current is also zero. Applying this to the set of equations (4.3), eliminates the last equation. This means that the 4 equations shown by (4.1) and (4.2) have now been reduced to only the 2 equations (4.4), containing the same information. This will significantly simplify the design of the controller.

4.1.2 Control loop regulating the power flow

The goal of the control loop is to govern the power flow to the grid. The instantaneous active power flow depends algebraically on the line-to-line voltage and current at the grid tie. The line-to-line voltage at the grid tie is external to the control system. Therefore, controlling the power injected in the grid is equivalent to controlling the current injected into it.

In the dq0 reference frame, the active and reactive power are defined as shown by (4.5). The classical definitions for active and reactive power are only defined for symmetrical, perfectly sinusoidal waveforms. A power invariant dq0 transform gives the same value as the classical definitions under these specific conditions. If the transform is not invariant for power, then the values will differ by a constant factor. Inverting the equation (4.5) gives an expression for the current as a function of power and voltage (4.6). [39]

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_d & u_q \\ u_q & -u_d \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{4.5}$$

$$\Leftrightarrow \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{1}{v_d^2 + v_q^2} \begin{bmatrix} v_d & u_q \\ u_q & -u_d \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{4.6}$$

Through (4.6), a set point for the power corresponds to a value for i_d and i_q. The

current is related to the voltage at the output of the converter, as shown by equations (4.4). The current control loop will adapt the converter output voltage v_C in order to obtain the current set point.

There are several control techniques available to achieve this. The studies conducted by Bahrani et al. [17] [19] describe state-of-the-art control techniques. These control techniques provide superior axis-decoupling and are less sensitive to deviations in the model parameters. Studying these is beyond the scope of this thesis. Maharjan et al. develop a control system for an eneergy storage specifically, and suffice with a classical PI-controller [14] [10]. This thesis adopts the same high-level control strategy.

Equations (4.7) and (4.8) show the equivalent of equations (4.4) in the Laplace domain. The first term on the left-hand side introduces cross-coupling between the two equations.

$$V_{Cd} - V_{Sd} + \omega L I_q = (pL + R)\, I_d \tag{4.7}$$

$$V_{Cq} - V_{Sq} \underbrace{- \omega L I_d}_{\text{coupling}} = (pL + R)\, I_q \tag{4.8}$$

Intermediate variables u_d and u_q are introduced in order to decouple the equations. By setting these variables equal to the left-hand side of equations (4.7) and (4.8), both equations are decoupled in terms of u and i. equations (4.9) show the definition of u. Fig. 4.4 shows how the inside of the control block in Fig. 4.2 is implemented. The decoupling block shows the implementation of equations (4.9).

$$\begin{aligned} u_d &= v_{Cd} - v_{Sd} + \omega L i_q \\ u_q &= v_{Cq} - v_{Sq} - \omega L i_d \end{aligned} \quad \Leftrightarrow \quad \begin{aligned} v_{Cd} &= u_d + v_{Sd} - \omega L i_q \\ v_{Cq} &= u_q + v_{Sq} + \omega L i_d \end{aligned} \tag{4.9}$$

From the perspective of the PI-controller, this greatly simplifies the complexity. The transfer function from u_d to i_d is now simply given by equation (4.10). The same applies for u_q, with the appropriate variables. Fig. 4.5 shows the block diagram of the control system. The electrical system together with the decoupling block are now contained in the G_s block. (4.11) shows the two standard forms of the transfer function of the PI-controller.

$$\frac{I_d}{U_d} = \frac{\frac{1}{R}}{1 + p\frac{L}{R}} \tag{4.10}$$

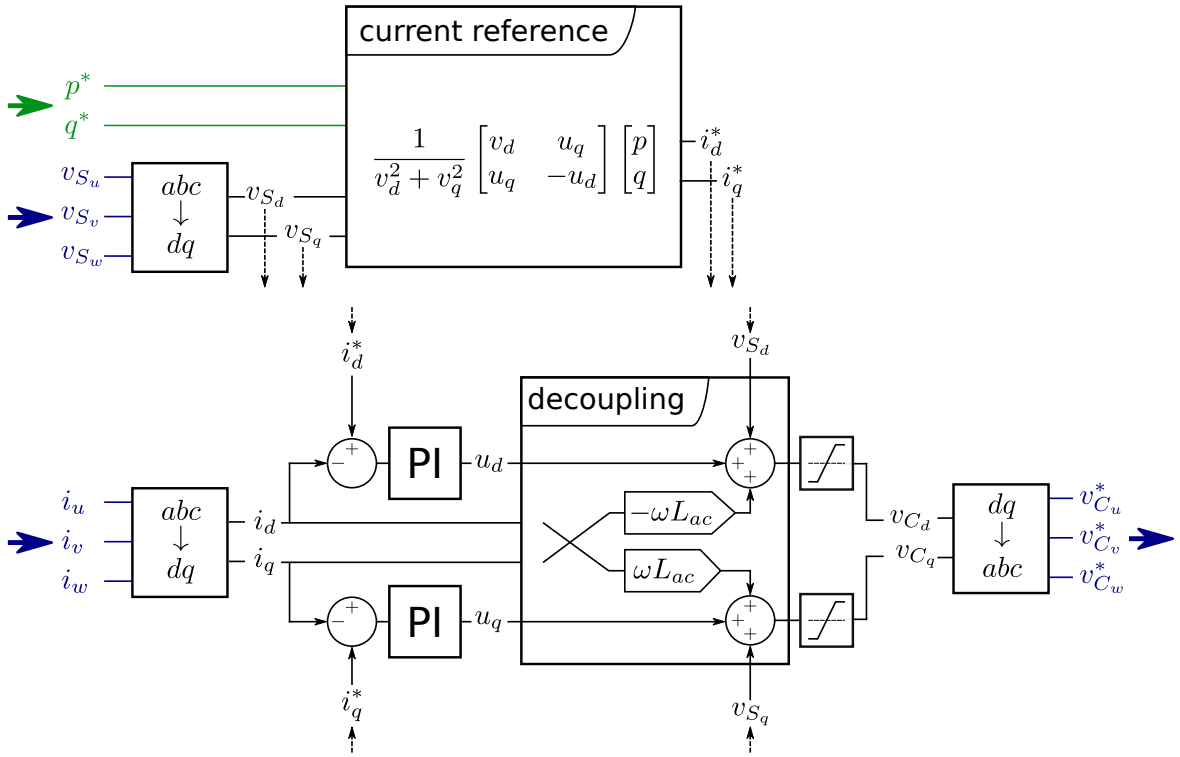


Figure 4.4: This figure shows the implementation of the inside of the control block in Fig. 4.2. The blue signals on the left are measurements taken in the electrical system, and the blue signals on the right go to actuators. The green signal is set as desired by a higher-level controller.

$$\frac{1+pT_n}{pT_i} = K_p + K_p\frac{1}{p} \qquad \begin{aligned} K_p &= \frac{T_n}{T_i} \\ K_i &= \frac{1}{T_i} \end{aligned} \tag{4.11}$$

The zero of the PI-controller is set equal to the pole of the transfer function of the system. This eliminates the pole in the open-loop transfer function as shown by (4.12).

$$G_o(p) = G_{PI}(p)\cdot G_s(p) = \frac{1}{pT_iR} \qquad T_n = \frac{L}{R} \tag{4.12}$$

The closed-loop transfer function is given by (4.13). The closed-loop system is a first-order system. The dynamic response of such a system is well-known. A step change in the input will cause the output to follow, where the error will decay exponentially. The exponential decay of the error is characterized by the time constant τ.

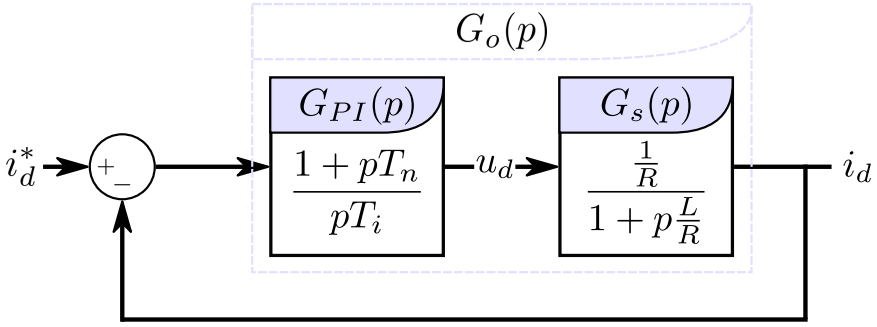


Figure 4.5: The system block G_s represents the dynamics of u_d to i_d; it includes the decoupling block and the electrical system. Exactly the same block diagram applies for the q-quantities, with appropriate names.

$$G_c(p) = \frac{1}{1+\frac{1}{G_o(p)}} = \frac{1}{1+pT_iR} \qquad \tau = T_iR \tag{4.13}$$

By eliminating the pole of the system, the PI-controller has one remaining degree of freedom, T_i. This parameter directly affects the time constant of the closed-loop system. It can be set to obtain a desired response to a step in the input signal. In this context, it is important to keep in mind that the analysis so far regarded the converter as in deal voltage source. In reality, the converter is a non-linear device which introduces a delay in the loop. This effect becomes significant for small time constants.

4.2 Converter operation

Fig. 4.6 shows the converter block. It receives a voltage reference for each phase from the interface and control layer. The converter operation layer then operates the inside of the converter block in such a a way as to achieve the desired voltage at the output of the converter.

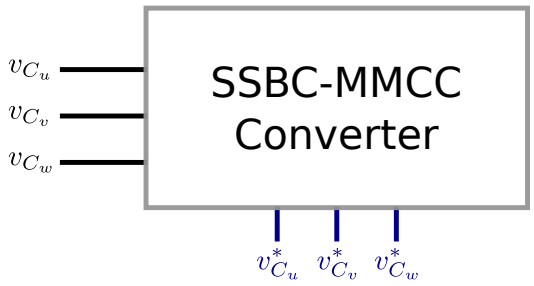


Figure 4.6: The converter receives a reference voltage for each phase from the control loop, indicated in blue. The converter operation layer tries to realize these voltages at the output of the converter, indicated in black.

This section consists of two subsections. The first subsection describes the hardware and structure of the converter. The second subsection describes the operation of the converter and how it achieves the desired output voltage. The converter operation layer assumes the switches to be ideal; they change state instantaneously and have no resistance. Only the next section which deals with the bottom layer, will introduce real switches.

4.2.1 Converter hardware

This thesis studies a specific converter design: the single star bridge cell (SSBC) modular multilevel cascaded converter (MMCC), hereafter referred to as the SSBC-MMCC converter. Fig. 4.7 shows the full layout of the converter. At the highest level, it consists of three clusters, one for each phase, which are connected in star-configuration. This explains the single star (SS) part of the name, contrasting it to topologies which are connected in delta and ones which have two stars. Each cluster in turn consists of several cells connected in series. The bridge cell (BC) part of the name specifies the type of these cells. Finally, the MMCC refers to the modularity of the converter which arises from connecting several cells in series.

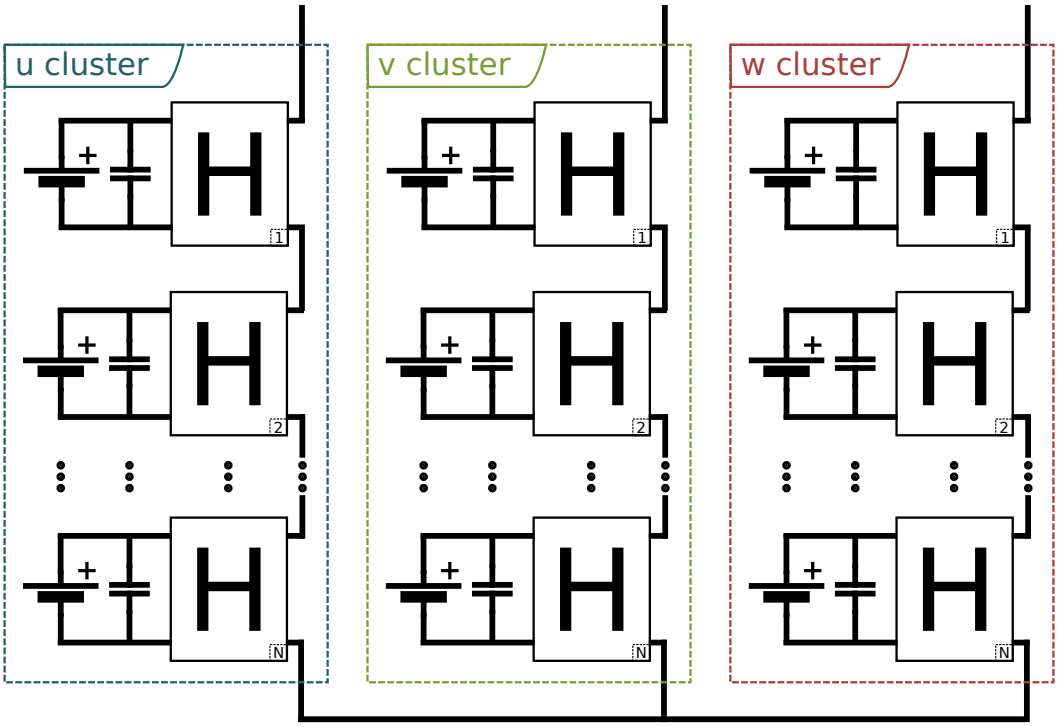
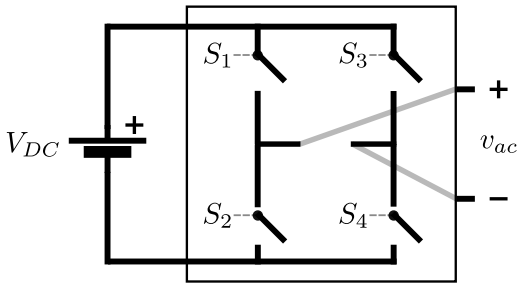


Figure 4.7: The converter consists of three clusters, one for each phase. A battery module is connected behind a H-bridge cell, in parallel with a capacitor. The combination of these three components forms the building block for each cluster.

The SSBC-MMCC converter is modular. It is easy to understand the operation of the full converter starting from its modules, the cells. Each cell consists of a battery, capacitor and an H-bridge. When a battery is charged, its state of charge (SoC) changes. The output voltage of batteries depends on the SoC, but stays relatively constant over the full range [15]. Especially over the duration of a switching period, the voltage change is negligible. This thesis will consider the battery as an ideal voltage source. The current drawn by the parallel capacitor is then zero, and doesn't affect the waveforms.

Figure 4.8a shows the idealized battery together with an H-bridge using 4 ideal switches. The output voltage level v_{ac} depends on the switching states, as shown by Table 4.8b. The cell can output three different voltage levels: V_{DC}, 0 and $-V_{DC}$. The switches in one leg are never turned on at the same time, because this would result in short-circuiting the battery.



(a) Schematic

S_1	S_2	S_3	S_4	v_{ac}
1	0	0	1	V_{DC}
1	0	1	0	0
0	1	0	1	0
0	1	1	0	$-V_{DC}$

(b) Switching states

Figure 4.8: The switching states give rise to different output voltage levels. S_1 and S_2 are never on at the same time to prevent short-circuit. Neither are they both off, because there has to be a path for the current. The same applies for S_3 and S_4.

4.2.2 Modulation

The converter operation layer has to control all the switches in the converter to obtain the desired output characteristics. The takeaway point from the hardware section is that each cluster consists of N cells in series, and each cell can at a given time output three voltage levels: V_{DC},0 and $-V_{DC}$. This leads to $2N+1$ levels for the entire cluster, ranging from $-NV_{DC}$ to NV_{DC}.

But the reference signal passed to each cluster will take on values in between these available levels. Pulse-width modulation (PWM) allows each cell to obtain any voltage at its output in the range $[-V_{DC}, V_{DC}]$, offering a solution to this limitation. PWM achieves this by quickly switching between different voltage levels of the cell, causing the average output voltage to take on the desired value. For a single cell, there are two main variants of PWM: bipolar and unipolar. Unipolar has superior characteristics when it comes to harmonics. Maharjan et al. choose this modulation technique in several studies [14] [10] [16]. This thesis will adopt unipolar PWM.

Fig. 4.9 shows the working principle of unipolar PWM (U-PWM). The switching state signals are generated by comparing a triangular trigger v_{trig} to a reference v_{ref}. The trigger has a frequency f_{sw}, hereafter referred to as the switching period. When the trigger crosses v_{ef}, then the state of both S_1 and S_2 will change. S_3 and S_4 on the contrary change when the trigger crosses $-v_{ref}$. This leads to the ouput wavefom shown by Fig. 4.9. Equation (4.14) shows how by varying the reference signal, the average output voltage can be controlled. The waveform repeats twice in a single switching period due to the nature of U-PWM. This means that in the frequency spectrum of the output voltage, all odd harmonics are eliminated. This is a desirable characteristic of U-PWM, and the reason why it is preferred over bipolar PWM.

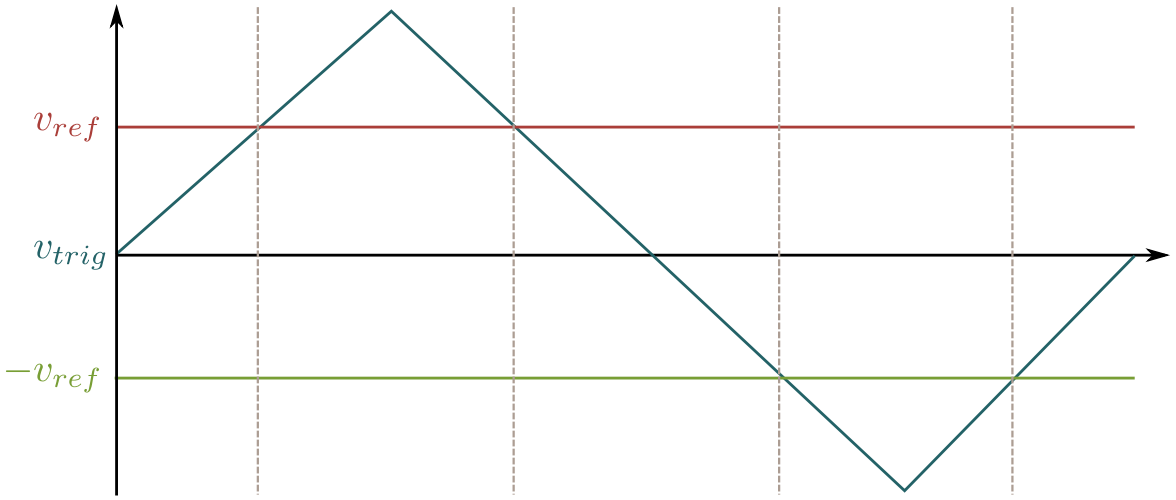
$$\langle v_{ac} \rangle_{sw} = \frac{v_{ref}}{\hat{v}_{trig}} V_{DC} \tag{4.14}$$

PWM allows each cell to obtain an output voltage in the range $[-V_{DC}, V_{DC}]$. Linking N cells together in series allows the cluster to reach an output voltage in the range $[-V_{DC}, V_{DC}]$. There are multiple ways to achieve this. For example, if the desired output of the cluster is V_{DC}, then cell 1 could provide this with all others being set to zero. Or, the first two cells could each provide exactly half of V_{DC}. This degree of freedom can be used to balance the SoC of the batteries linked to each cell [40] [15].

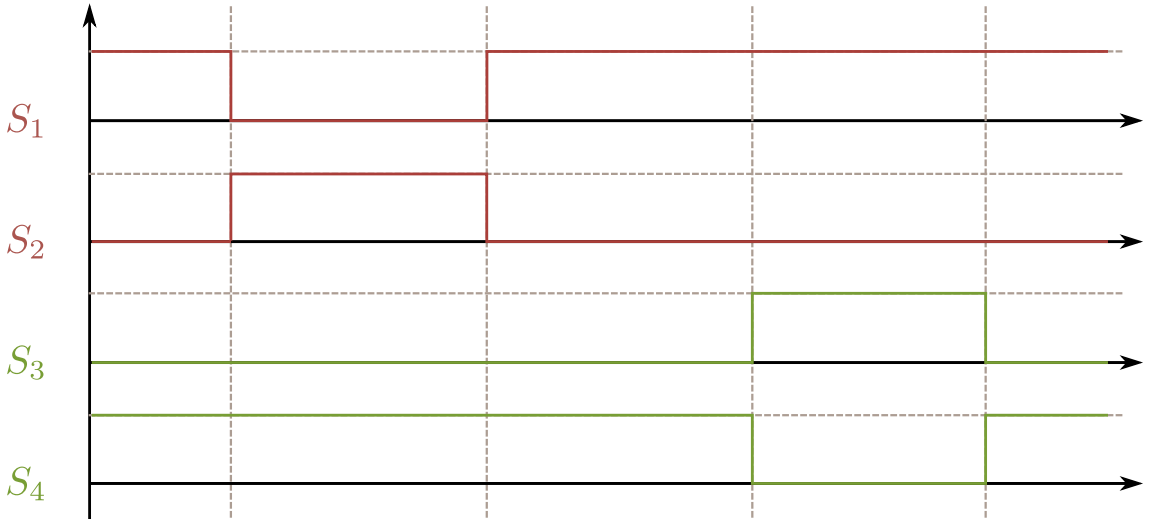
There are two main types of methods to coordinate the cells in a cluster: carrier disposition and sub-harmonic methods [20]. Each has a distinct advantage. Carrier disposition methods divide the full available range $-NV_{DC}$ to NV_{DC} in N bands, of width $2V_{DC}$. Within each band, only one cell is being switched. All other cells have a constant output voltage. As the total output voltage increases, the active cell increases its output voltage, until it reaches V_{DC}. At that point, another cell which was previously outputting 0, takes over. This method leaves a degree of freedom as to which cell is activated when the trigger leaves the previous band. The main advantage of this method is that only one cell at a time is switching, improving the lifetime of the switches.

The sub-harmonic method on the other hand reduces the harmonics in the output waveform. All cells are active at the same time, and take on an equal share of the cluster voltage. For example, if the desired cluster voltage is $\frac{V_{DC}}{2}$, then each cell will output $\frac{V_{DC}}{2N}$. The triggers of the cells are phase-shifted by $\frac{360\circ}{N}$. This thesis adopts the sub-harmonic method. Therefore, the next paragraph will explain in detail the harmonic elimination due to this method.

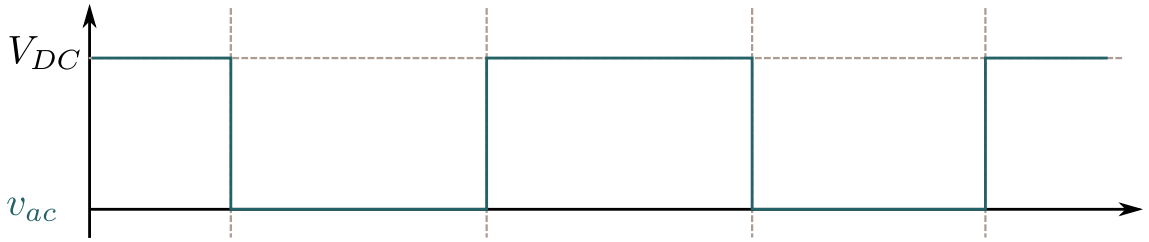
The reference signal is in steady-state operation sinusoidal with the same frequency as the grid, f_n. The switching frequency is typically significantly larger than the grid frequency. Approximately, in a single switching period, the reference signal stays constant. With this approximation in a short time period, the waveforms of cells 2 to N are identical to the waveform of cell 1, but phase-shifted. Equation (4.15) proves that the cluster waveform v_c is periodic with period $\frac{T_{sw}}{N}$. This implies that only harmonics which are a multiple of Nf_{sw}, are present in the cluster waveform. In reality, the waveforms of the cells differ slightly due to the small change in the reference signal. There will be some harmonics present, but they will be strongly reduced.



(a) Trigger and reference signal



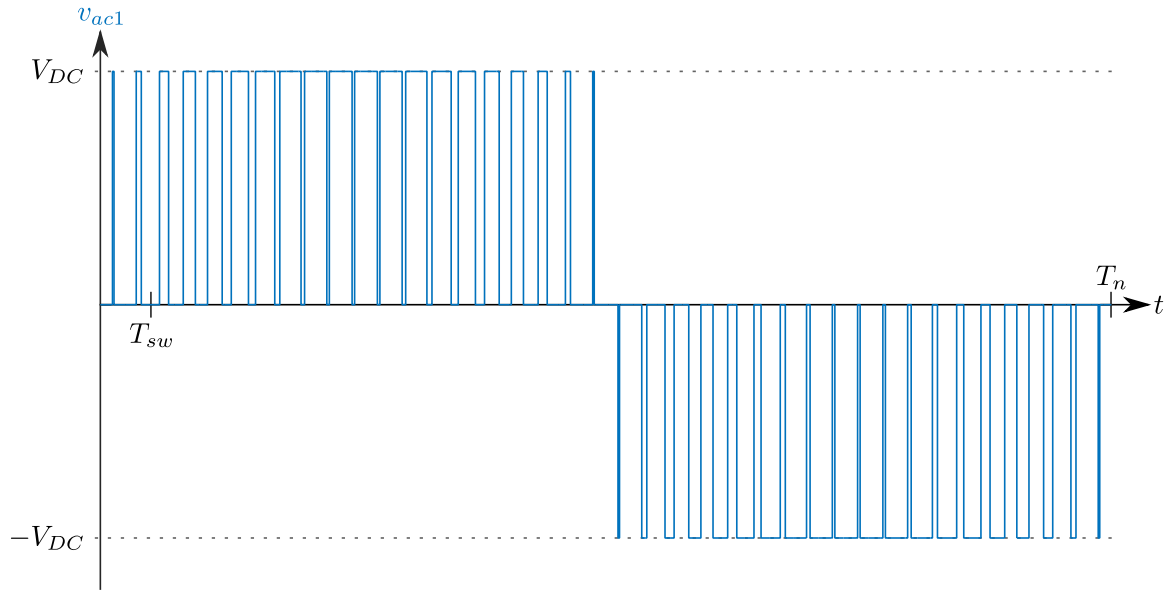
(b) Switch state signals



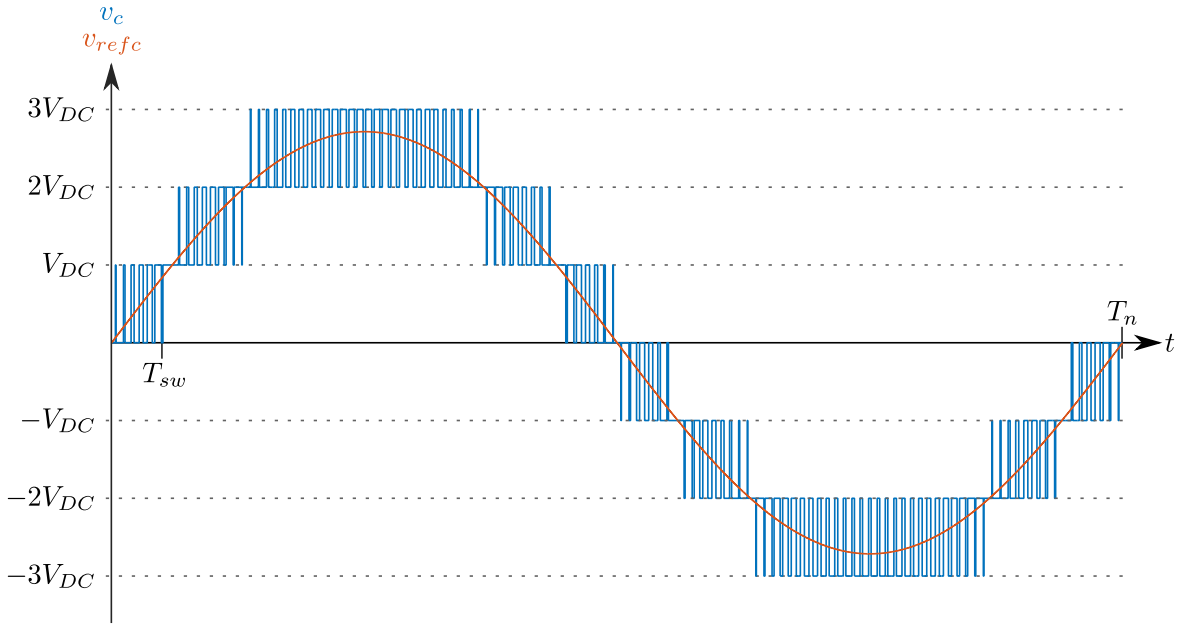
(c) Resulting output voltage

Figure 4.9: This figure shows the working principle of unipolar PWM of a single cell. Fig. 4.8 shows how the switching states in 4.9b lead to the voltage levels in 4.9c.

$$
\begin{aligned}
v_c(t) &= \sum_{n=0}^{N-1} v_{ac,n}\left(t + n\frac{T_{sw}}{N}\right) \\
v_c\left(t + \frac{T_{sw}}{N}\right) &= \sum_{n=0}^{N-1} v_{ac}\left(t + [n+1]\frac{T_{sw}}{N}\right) \\
&= v_{ac}\left(t + N\frac{T_{sw}}{N}\right) + \sum_{n'=1}^{N-1} v_{ac}\left(t + n\frac{T_{sw}}{N}\right) \\
&= \sum_{n'=0}^{N-1} v_{ac}\left(t + n\frac{T_{sw}}{N}\right) \\
&= v_c(t)
\end{aligned}
\tag{4.15}
$$



(a) Output waveform of the first cell



(b) Aggregate waveform of the whole cluster, with the reference signal

Figure 4.10: The waveform of the entire cluster is the aggregate of the waveforms of the individual cells. This Figure shows the waveforms for a cluster with three cells, $N = 3$, and a specific ratio for the periods, $\frac{T_p}{T_{sw}} = 20$. The converter is slightly oversized; the range of the converter is larger than the range of the reference signal.

4.3 Loss model

Up until this point, there are no losses present in the model. The top and middle layer control the converter, and do not consider the losses. But the losses are a very important aspect, justifying choosing one converter over another. This section describes the bottom layer, the loss model.

The losses are caused by the switches. There are two main types of losses: conduction losses and switching losses [38]. When real switches are closed, they cause a small voltage drop across their terminals. By conducting current at the same time, they consume an amount power which leaves the converter as heat. These are the conduction losses. The switching losses are a consequence of the finite switching time of real switches. When the switch changes state, it needs a certain amount of time to realize the change of state. For example, when the switch closes, the voltage across it has to drop and the current through it increases. These two changes happen at the same, and incur a loss, the switching loss.

Fig. 4.12 shows the switch models used in this thesis. The first two layers use ideal switches, shown by Fig. 4.12a. In reality, a switch consists of an IGBT in parallel with a freewheeling diode, shown by Fig. 4.12b. The IGBT takes care of the actual switching, whilst the diodes are necessary because of the finite switching time. The dynamics of both semiconductor devices will determine the losses incurred during switching, whilst the conduction losses are a function of the transfer characteristics.

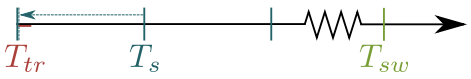
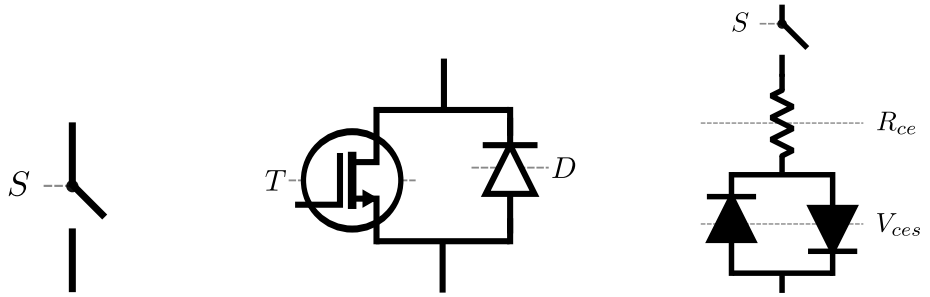


Figure 4.11: The transient dynamics of the switches take place in a much smaller timescale T_{tr} than the switching period T_{sw}. In order to capture the transient dynamics, the solver has to take substantially smaller time steps as indicated by the dashed arrow.

The dynamic behaviour of the IGBT and diode determine the switching losses. The time required to change the state of a switch is typically in the order of $1\mu s$, whilst the switching period is typically three orders of magnitude larger. As shown by Fig. 4.11, the time step should be lowered substantially in order to capture the transient dynamics of the switches. This would result in a substantially slower simulation. This thesis therefore opts for an event-based model of the switches. Furthermore, the datasheets characterizing the devices are not detailed enough to provide an accurate dynamic model. Implementing the computational costly model doesn't guarantee a more accurate result.

This section contains two subsections. The first subsection will describe the dynamics of the semiconductor switch. Understanding the dynamics is essential to develop an accurate event-based model, replacing the direct simulation of the dynamics. The second subsection deals with the event-based model itself.



(a) Ideal switch (b) IGBT and diode (c) IGBT model

Figure 4.12: The first two layers of the model use an ideal switch. In reality, the switch consists of an IGBT and a diode. The conduction losses are included in the dynamic model finally as shown by Fig. 4.12c.

4.3.1 Modeling the semi-conductor losses

The first two layers consider the IGBT to act as an ideal switch. But in reality, the IBGT is a three-terminal device which requires a finite time to realize a change in state [41]. There are several physics-based models of IGBTs, aiming to accurately represent the dynamic behaviour [30] [36] [32] [42]. Not only are these models computationally expensive, the parameters of these models are hard to extract from the data sheets alone. Lauritzen et al. [31] aim to offer an easy parameter extraction for their model. But in doing so, they make some additional assumptions. These models tend to be quite complicated, and using them in practice requires additional simplifications because of limited available data. Therefore, this thesis adopts another approach.

Another approach is what this thesis will refer to as the algebraic model. The switching waveforms of the IGBT mostly depend on the voltage and current levels, which are dictated by the H-bridge operation. Qualitative knowledge of the dynamics is essential to justify the assumptions made in the algebraic approach.

IGBTs need a certain amount of time to turn on or off, t_{on} and t_{off}. Therefore, switching the IGBTs in a single leg cannot be done at the same time; this would create a short-circuit in the battery. Fig. 4.14a for example shows the commutation of the left leg. The upper switch turns off first at t_1. But because of the inductive load, the

current cannot change. Therefore, a freewheeling diode in that leg will take over the current, depending on the current direction. Both IGBTs in the left leg are now turned off. Next, the other IGBT turns on at t_2, taking over the current from the freewheeling diode. Subsection 4.3.2 discusses these sequences in greater detail.

The key point is that an IGBT always takes over the current from a freewheeling diode when it turns on. The diode itself turns on almost instantly, but the turn-off causes some significant losses compared to the turn-on. These losses are known as the reverse recovery losses. The diode consumes negative current in the final stage of turning-off, to remove the remaining charge in its junction. This reverse recovery current will affect the transient waveforms of the IGBT when turning on. Based on these type of operating considerations, Rajapakse et al. [29] develop formulas which give the switching losses of both diode and IGBT. A similar approach is used by other authors [43] [38] [33].

The formulas developed by [29] depend on datasheet parameters and operating conditions of the H-bridge, the battery voltage and the load current at time of switching. These formulas contain many terms, due to the piece-wise nature of the approximate waveforms. When applied, it turned out that not all parameters were available in the datasheets of the devices. Instead, this thesis adopts a more straight-forward approach. The datasheets of the IGBT and diode contain graphs of the switching losses versus the load current at a specified voltage V_{ref}. Dieckerhoff et al. [34] use equation (4.16) to model the current and voltage dependency of the switching loss. The parameters a,b and c are the result of a quadratic fit of the datasheet graphs. The same equation is suggested by the IGBT manual of ABB, a major IGBT producer [35]. This thesis uses this equation to model the depency of the turn-on, turn-off and reverse recovery losses.

$$E_{sw} = \frac{V}{V_{ref}} \left(a \cdot I^2 + b \cdot I + c \right) \tag{4.16}$$

4.3.2 Event-based model

The event-based model offers an alternative to simulating the full dynamics of the switches. The same approach is adopted by Kouro et al. [33], besides that this thesis uses equation (4.16) to model the voltage and current dependency of the switching losses.

Fig. 4.13 shows the switching signals of the U-PWM, augmented with a blanking

time t_{blank}. This blanking time is necessary to prevent short-circuits; it guarantees that the closing switch has enough time to completely close, before the other IGBT starts to open. The direction of the load current determines which freewheeling diodes will conduct during the leg commutation. Table 4.1 gives a full oversight of which devices are changing state at which moment. Take for example time instance t_1. The upper IGBT in the left leg switches off. But due to the inductive load, the current finds a new path. Depending on the current direction, either the upper or lower diode provides a path for the current. If the upper diode switches on, then nearly no voltage build-up occurs across the IGBT. But if the lower diode switches on, a voltage builds up across the IGBT and induces a significant switching loss. Fig. 4.14 shows a graphical representation of the events for a positive load current.

Whenever a switching event occurs due to the converter operation, Table 4.1 indicates which devices change state as a consequence of this. By measuring the voltage and current at that time, equation (4.16) allows for the calculating of the switching loss in each device. This is purely algebraic, and computes significantly faster than a dynamic model of the switches.

So far, the conduction losses were not discussed. An ideal switch has no voltage across its terminals when it is closed. When it is open, it blocks all current. A real switches does both of these. But in terms of power loss, only the closed state is of importance. The conduction loss then simply follows from the transfer characteristic. The data sheet typically contains a graph of this characteristic. This thesis approximates the graph with an electrical circuit containing a constant voltage drop and a linear resistance. Section 5.1 explains the parameter extraction in detail. The conduction loss of the diode is insignificant compared to the conduction loss of the IGBT. The diodes only conducts during the blanking interval, whilst the IGBTs conduct during the remaining timeslots in the switching period. Since the blanking interval is typically much smaller than the switching period, the diode conduction losses are neglected.

By including the circuit shown by 4.12c, the conduction losses are included in the dynamic simulation of the converter as a whole. The switching losses are calculated separately, adding to the total switching losses whenever a switching event occurs. The effect of voltage and current at time of switching is taken into account.

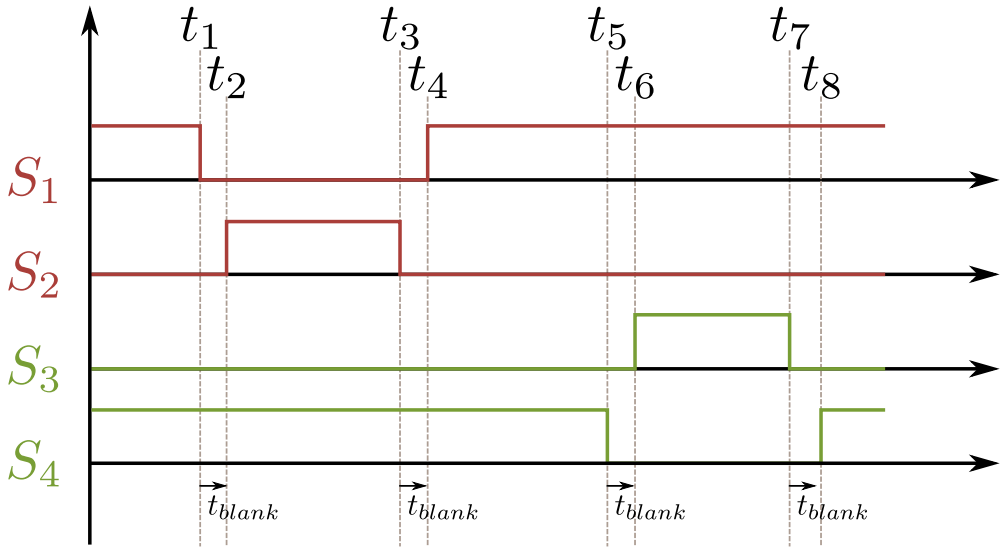
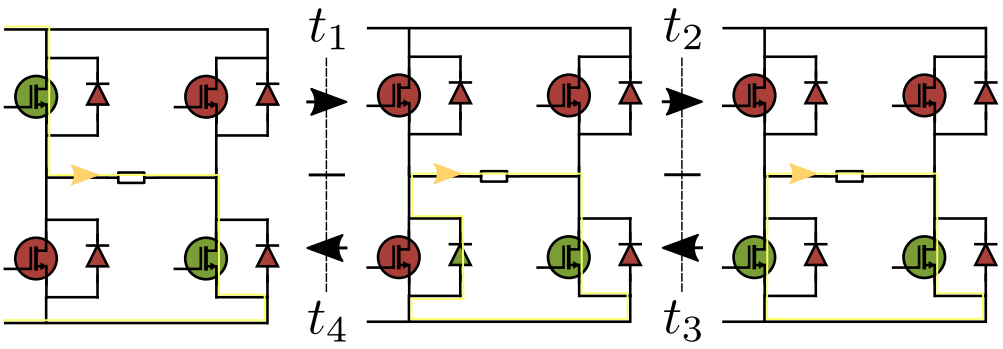
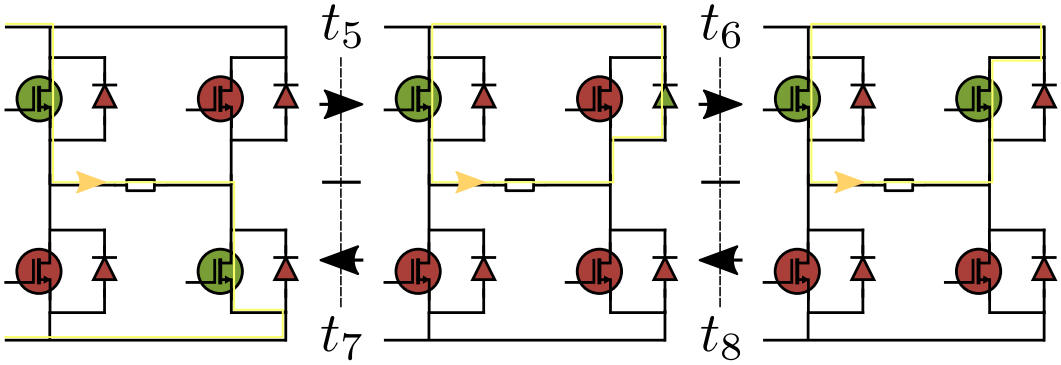


Figure 4.13: The blanking time t_{blank} guarantees that the closing switch has enough time to completely close, before the other IGBT starts to open. A short-circuit would occur if this was not in place.



(a) $t_1 \rightarrow t_4$



(b) $t_5 \rightarrow t_8$

Figure 4.14: The load current finds a path through the converter at all times. During the blanking interval, when both IGBTs are eventually turned off, a freewheeling diode provides a path in the commutating leg. This Figure shows only the commutation for a positive load current, corresponding to Table 4.1a.

Chapter 5

Case study

This chapter will apply the developed model to a specific use case. This is an important step towards reaching the objective of the thesis. In addition to developing a conceptual model of the converter, an actual tool is implemented based on it. This tool is then used to simulate a specific use case. The results of this simulation then enable further analysis, demonstrating the potential of the tool.

The first section presents the input data. This includes things such as nominal ratings of the converter, semiconductor components etc. The second section presents the tool and a base case. This base case forms a starting point from where the design can be explored. The three last chapters extensively use the tool to analyze key performance indices (KPI) such as harmonics, losses and reliability. In doing so, they change the base case to examine how certain parameters affect these KPI.

5.1 Data

5.1.1 Converter ratings

The specifications of the converter are set to typical values for converters applied in the power network, fitting the research interests of CITCEA. The nominal power of the converter is 100kW. 9 battery modules are available, at a nominal voltage of 350V each. The short circuit power absorbed by the converter is allowed to be 1% of the nominal power, and the short circuit impedance should be not lower than 10% of the nominal one. Table 5.1 summarizes these parameters.

The AC phase voltage follows from the modulation strategy and number of batteries connected in series in a phase. Each module is controlled by unipolar PWM. Since there

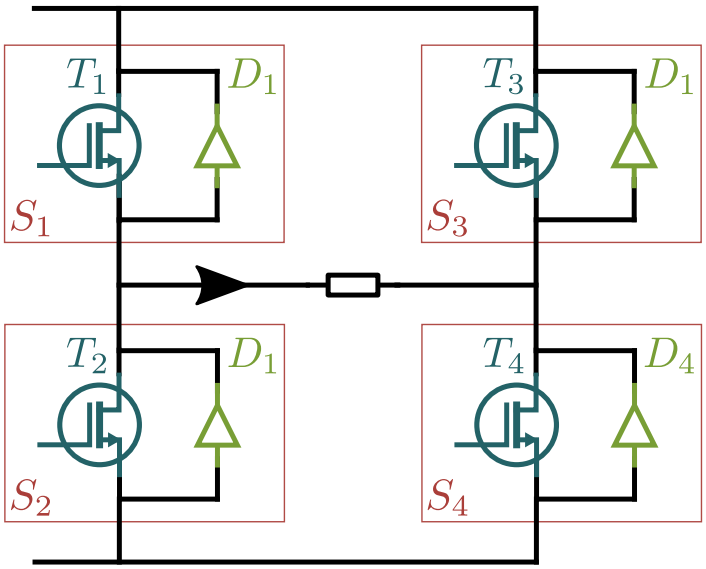


Figure 4.15: A real H-bridge has 4 diodes and IGBTs.

Table 4.1: These tables indicate the switching events for all semiconductor devices under U-PWM as shown by Fig. 4.13. Fig. 4.15 shows the location of the devices within the H-bridge. The diode turn-on power loss is negligible compared to the other events, and is indicated in light gray. Furthermore, only the events indicated in boldface cause significant losses.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
T_1	**OFF**			**ON**				
D_1								
T_2		ON	OFF					
D_2	ON	OFF	ON	**OFF**				
T_3						ON	OFF	
D_3					ON	OFF	ON	**OFF**
T_4					**OFF**			**ON**
D_4								

(a) Positive current

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8
T_1	OFF			ON				
D_1	ON	**OFF**	ON	OFF				
T_2		**ON**	**OFF**					
D_2								
T_3						**ON**	**OFF**	
D_3								
T_4					OFF			ON
D_4					ON	**OFF**	ON	OFF

(b) Negative current

Table 5.1: The ratings of the converter are set to typical values for converters applied in the power network.

Parameter	Value
S_{rated}	$100kW$
V_{DC}	$350V$
P_{SC}	$0.01P_{rated}$
Z_{SC}	10%

are 9 battery modules in total, 3 battery modules are connected in series in a single phase. The modulation index is lower than 1 to prevent saturation of the controller when there is some ripple in the reference voltage. With a modulation index m_a of 0.9, the resulting AC phase voltage is

$$V_{AC,f} = \frac{3m_a V_{DC}}{\sqrt{2}} = 668V \tag{5.1}$$

The current rating follows from the power and voltage rating

$$I_{AC} = \frac{S_{rated}}{3V_{AC,f}} = 50A \tag{5.2}$$

5.1.2 Semiconductor components

Each H-bridge consists of 4 IGBT modules, consisting in turn of an IGBT and a free-wheeling diode. The IGBT module FS100R17KE3 produced by infineon provides the required voltage and current handling capabilities. The full datasheet is attached in Appendix A.1. This subsection will focus on how the relevant model parameters were extracted from this datasheet. The specifications of the IGBT module is the determining factor for the switching and conduction losses. Therefore, a good approximation is essential for the correct representation of the losses. are set to typical values for converters applied in the power network

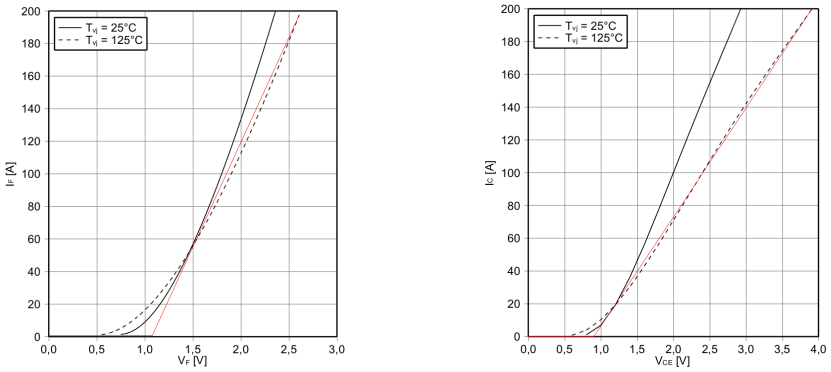
Transfer characteristics

The transfer characteristics determine the conduction losses of the components. Fig. 5.1a and 5.1b show the transfer characteristic of respectively the diode and the IGBT. The developed model does not include a thermal model. Therefore, the characteristics at $125°C$ were used, to obtain the worst-case losses. The effect of the gate voltage is not considered. Both the IGBT and the diode have an exponential transfer characteristic.

This can be approximated electrically by an ideal diode causing a constant voltage drop in series with a linear resistance. This representation is often used for real diodes. Fig. 5.1a and 5.1b show the resulting characteristic of the approximation with a red line. Table 5.1c gives the numerical values corresponding to these fits.

Switching losses

The current dependency of the switching losses is shown by Fig. 5.2a and 5.2b. The relation between both is approximately quadratic, and was therefore approximated by a quadratic fit. Table 5.2c shows the coefficients obtained by a least-square quadratic fit of several points along the curve. The resulting approximate curves are shown in color in Fig. 5.2a and 5.2b.

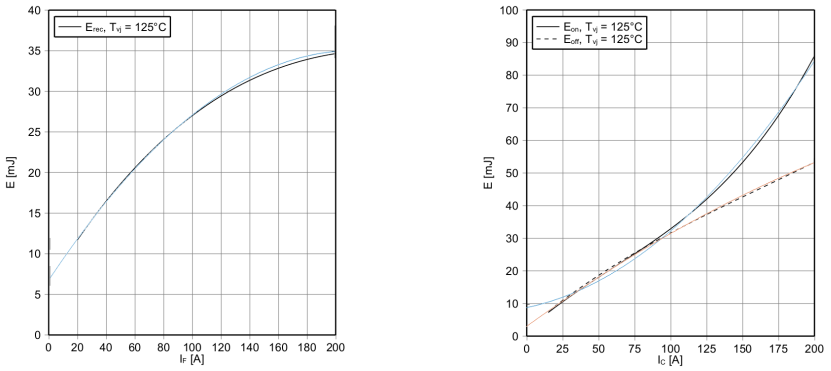


(a) Diode (b) IGBT

Diode		IGBT	
V_f	$1.083V$	V_{ces}	$0.923V$
R_f	$7.638m\Omega$	R_{ce}	$13.01m\Omega$

(c) Coefficients of the fitted approximation.

Figure 5.1: The transfer characteristic of the diode and IGBT is fitted by a constant voltage drop and a linear increase increase thereafter. The red line shows the resulting approximation.



(a) Diode (b) IGBT

	a$[J/\sqrt{A}]$	b $[J/A]$	c[J]
E_{on}	1.4234E-6	9.0802e-05	0.090
E_{off}	-3.3093e-07	3.1626e-04	0.033
E_{rec}	-6.1590e-07	2.6327e-04	0.0070

(c) Coefficients of the fits

Figure 5.2: The switching losses show a quadratic dependency with respect to the current. The blue and red curve show the results of the quadratic approximation of the real curves.

5.2 Simulation tool

This section presents the implemented tool. First, the used simulation framework is discussed. Secondly, the base case is presented. The base case is an initial implementation of the converter, ignoring aspects such as harmonics and reliability. It forms a starting point for further analysis. Some design choices will be iterated upon in later chapters to improve the performance of the converter. Finally, some results of the base case are presented.

5.2.1 Simulation framework

The tool is implemented in the software suite provided by MathWorks, consisting of two main products: Matlab and Simulink. The tool makes use of both. Matlab includes a programming language, compiler, console and a GUI which ties everything together. Its syntax is very well suited for matrix operations, making it a convenient tool for quick prototyping. Simulink on the other hand is a multi-domain simulation environment. It is a graphical solution in the sense that the modeling language consists of blocks, which are connected together to create complete systems. Simscape, a toolbox available for Simulink, provides additional blocks for physical systems. Several physical domains are included: electrical, pneumatic, mechanical... It is also possible to define custom blocks, extending the modeling language [44].

Fig. 5.3 shows the structure of the tool, operating as a black box between a set of inputs and outputs. The tool consists of two main files: a parameter script and a model file. Appendices B and C contain the implementation of the script and model. The parameter script contains input parameters for the model. These can be classified in four categories: sizing, component, time and control. The sizing parameters contain the high-level specifications of the converter: rated power, rated voltage, grid frequency, short-circuit power... It corresponds to the parameters discussed in subsection 5.1.1. Additionally, it calculates an initial sizing of the filter based on the short-circuit limitations. The component parameters are taken from the datasheet in Appendix A.1. For the transfer characteristics, series of V-I points are included. The script converts these to a quadratic fit. The time category defines all time constants: switching frequency, simulation step time etc... Finally, the control section tunes the PI-controllers of the current loop.

The model file contains the physical description of the converter and the control system. By connecting blocks together, a representation of the entire converter is

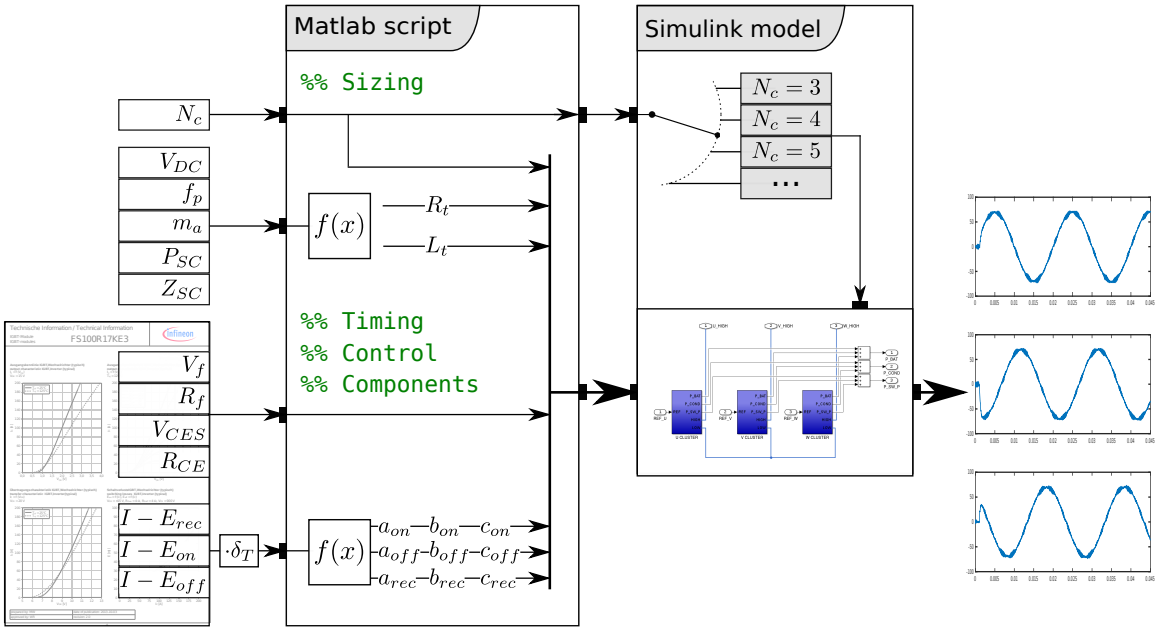


Figure 5.3: The semiconductor datasheet and several sizing parameters provide the input for the Matlab script file. The script processes this data together with some initial calculations, and passes it to the Simulink model. The cascade number N_c changes the required layout of the model, which makes it distinct from all other parameters. The model outputs the waveforms to Matlab.

created. Low-level blocks are grouped in subsystems which have inputs and outputs. These subsystems are then reused to form even more complex subsystems. The highest level represents the interface and control. The cluster subsystem belongs to the converter operation layer. The cell subsystem belongs to the two bottom layers, since it contains both the ideal switches and the representation of switching and conduction losses. Blocks can contain parameter names instead of values, creating an interface with Matlab. Only the cascade number N_c can not be represented as a parameter in Simulink. It dictates how many times the cell subsystem should be repeated.

The work flow of a single simulation run goes as follows. Firstly, the parameter script is executed, populating the Matlab environment with the parameters contained in the script. Secondly, the simulation of the model file starts. Before the solver starts to simulate the model, Simulink reads the parameters contained in the Matlab environment. When the solver finishes, Simulink writes the results of the simulation to parameters in the Matlab environment, according to instructions in the model file. A higher level script can execute this work flow repeatedly, overwriting some parameter and collecting the results of each simulation run. For example, in the next sections, this is done for the inductance of the filter and for the rated power output. Varying the

cascade number N_c requires a more elaborate scheme with a new model file for each value.

5.2.2 Base case

Subsection 5.1.1 already listed some high-level specifications of the converter. The base case further includes an initial sizing of the filter. This is done according to the short-circuit requirements listed in Table 5.1. The converter is generating active power only. Therefore, the rated power is equal to the apparent power

$$P_{rated} = S_{rated} = 100kW \tag{5.3}$$

When the converter is short-circuited, the nominal current still flows through the resistance of the filter. This induces a short-circuit power P_{SC}. It is required that P_{SC} stays below the level specified by Table 5.1, leading to an upper limit for R

$$R \leq 3P_{SC}\left(\frac{V_{AC}}{P_{rated}}\right)^2 = 0.1340\Omega \tag{5.4}$$

Where V_{AC} is the phase voltage and not the line-to-line voltage. Additionally, Table 5.1 lists a requirement for the impedance in short-circuit conditions. The impedance increases with both the resistance and inductance in the filter. Assuming the maximum allowable value for R, this leads to a lower limit for the inductance

$$L \geq \frac{1}{2\pi f_n}\sqrt{\frac{3\left(V_{AC}\right)^2}{P_{rated}} - R^2} = 4.243mH \tag{5.5}$$

For the sake of clarity, the initial inductance size is set below this limit. This will make the harmonics more pronounced, and will facilitate their analysis.

$$L = 1.4mH \tag{5.6}$$

Eventually, after analyzing the harmonics, the value for the inductance will be increased, taking into account both the harmonics and the limit expressed by (5.5). In chapter 5.4, the inductance will be further tuned.

Finally, some time constant have to be specified. The grid frequency, switching

frequency and sampling frequency are

$$f_n = 50Hz \qquad f_{sw} = 1kHz \qquad f_s = 100kHz \tag{5.7}$$

The sampling frequency determines the time step taken by the solver. It is 100 times smaller than the switching frequency. This means that the resolution of one switching period is 100 samples. This is accurate enough to clearly display the switching waveforms. Increasing the sampling frequency further leads to longer simulation runs, and is therefore undesirable.

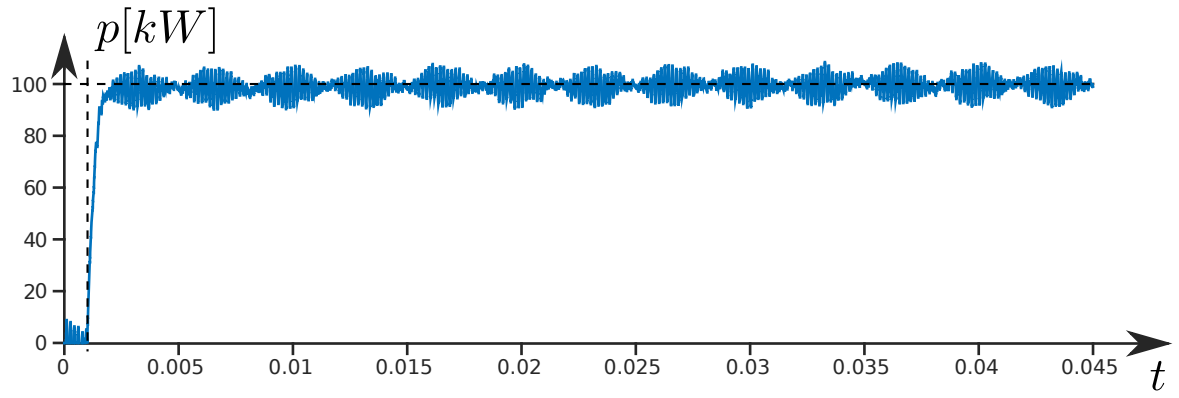
5.2.3 Initial results

The time constant of the PI-controllers was further tuned based on the simulation results. Lowering the time constant to

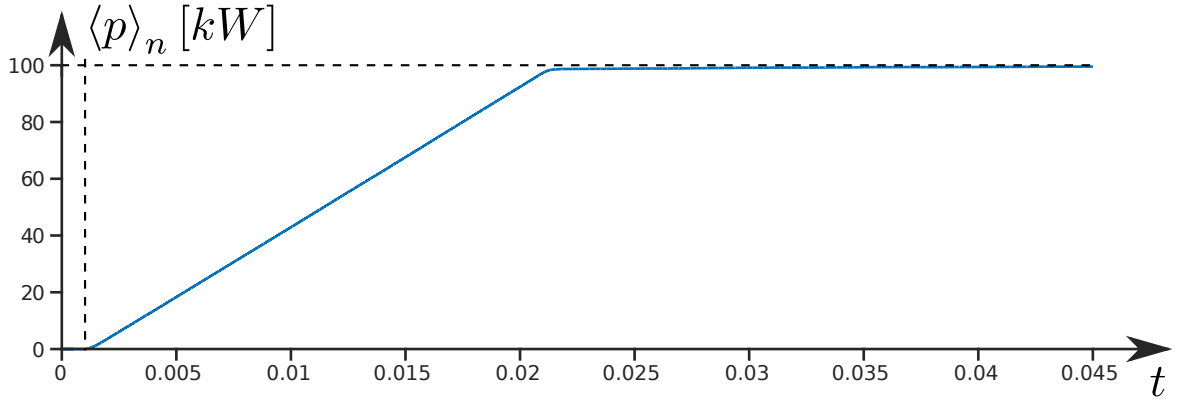
$$\tau = \frac{T_{sw}}{6} \tag{5.8}$$

gives a very fast response to a step change from no power output to full rated power. Fig. 5.4 shows the instantaneous power and the time-averaged value over one period of the grid frequency. One period T_n after the step change, the output power has nearly reached the desired value. This will be useful in further analysis when the steady-state waveforms are required. The simulation only has to run for two periods after the step change to obtain quasi steady-state operation.

Fig. 5.5 shows the current in each phase during the step change in the output power. The harmonics present in the converter voltage cause a ripple current, modulated on the fundamental sinusoidal current. Whether this level of ripple current is acceptable, will be discussed in great detail in section 5.4.

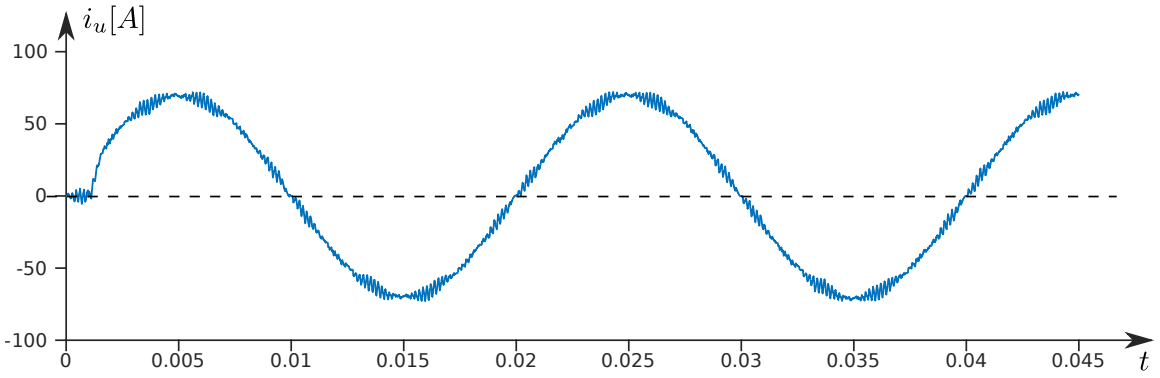


(a) Instantaneous power

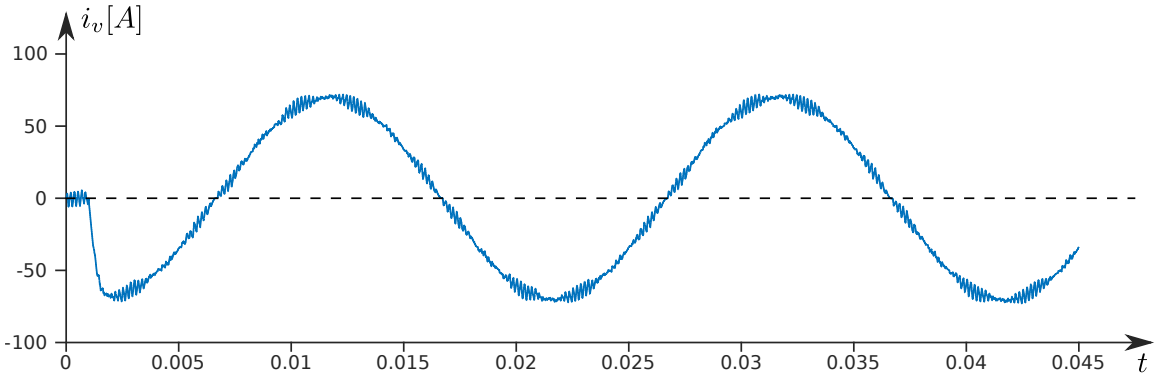


(b) Average power ($T = T_n$)

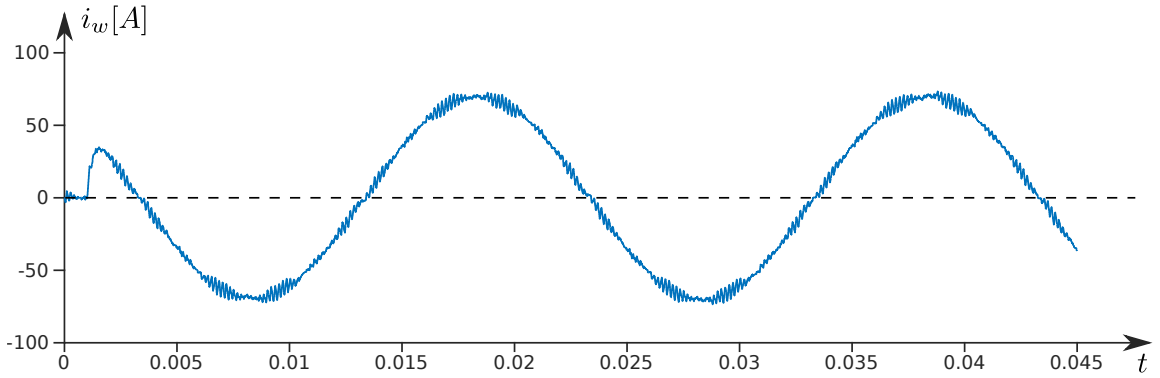
Figure 5.4: The power set point increases from $0kW$ to $100kW$ at $t = 1ms$. The controller makes the converter follow this change in input within the next $1ms$. The oscillations in the immediate power are due to the harmonics in the current waveform, but do not affect the average power.



(a) u-phase current



(b) v-phase current



(c) w-phase current

Figure 5.5: The current loop controller regulates the current by changing the converter voltage. The harmonics present in the converter voltage cause a ripple current, modulated on the fundamental sinusoidal current.

5.3 Power loss analysis

The losses are one of the key performance indicators which could motivate the choice for a specific converter. This analysis looks at the losses in the converter itself, due to imperfect switches and parasitic resistances. There is another important aspect when it comes to losses: harmonics. The harmonics enter the grid and induce losses in other devices. This harmonic loss is not included in this section. According to Kou et al., this is exactly one of the benefits of multilevel inverters; the reduced harmonics leads to lower losses [45].

This section examines the implications of the loss model discussed in section 4.3. First, approximate formulas are derived for the steady-state operation of the converter. The predictions obtained from these formulas are then compared with the simulated operation of the converter.

5.3.1 Analytic formulas

The losses in the converter are caused by the imperfect switches and parasitic resistance. These losses can be grouped in two classes: conduction losses and switching losses. This subsection will derive approximate formulas for both loss components during steady-state operation. Steady-state in this context means that the current waveform is periodic

$$i(t) = \hat{I} \sin(\omega t) = \sqrt{2} I \sin(\omega t) \tag{5.9}$$

If the converter is not generating any reactive power, then the current is simply related to the active power by

$$I = \frac{P}{3V_{AC}} \tag{5.10}$$

Conduction losses

The conduction losses are caused by the IGBTs and the filter. The voltage across the terminals of an IGBT increases with the current. The relationship between both is called the transfer characteristic. Since the voltage is non-zero, energy leaves the IGBT as heat. The transfer characteristic was approximated by

$$v_{IGBT}(t) = V_{CES} + R_{CE} \cdot |i(t)| \tag{5.11}$$

where V_{CES} is the collector-emitter on-state voltage drop and R_{ce} is a linear approximation of the current dependency of the total voltage drop. For steady-state operation, time-averaging the instantaneous power over one period gives a formula for the average power loss due to conduction

$$\begin{aligned}
\langle P_{cond,IGBT} \rangle &= \frac{1}{T} \int_0^T v_{IGBT}(t) \cdot |i(t)| \; dt \\
&= \frac{1}{T} \cdot \int_0^T V_{CES} \cdot |i(t)| + R_{CE} \cdot i^2(t) \; dt \\
&= \frac{2}{T} \int_0^{\frac{T}{2}} V_{CES} \cdot \hat{I} \sin(\omega t) + R_{CE} \cdot \hat{I}^2 \sin^2(\omega t) \; dt \\
&= \frac{2}{T} \int_0^{\frac{T}{2}} V_{CES} \cdot \hat{I} \sin(\omega t) + R_{CE} \cdot \hat{I}^2 \left[\frac{1 - \cos(2\omega t)}{2} \right] \; dt \\
&= \frac{2}{\pi} V_{CES} \cdot \hat{I} + \frac{1}{2} R_{CE} \cdot \hat{I}^2 \\
\Rightarrow \langle P_{cond,IGBT} \rangle &= \frac{2\sqrt{2}}{\pi} V_{CES} \cdot I + R_{CE} \cdot I^2
\end{aligned} \tag{5.12}$$

In each cell at any time, two IGBTs are conducting the current. During the blanking time, the diodes conduct the current, but since the blanking time is much smaller than the switching period, these losses are negligible. Each cell in a cluster conducts the same current, because they are connected in series. The current waveform is phase-shifted across the phases. This means that the instantaneous current is different, but the time-averaged value is the same. These three arguments justify that the total conduction loss is simply obtained by scaling (5.12) with the total number of IGBTs

$$\begin{aligned}
\langle P_{cond} \rangle &= (2 \cdot N_c \cdot 3) P_{cond,IGBT} \\
&= 6N_c \left[R_{CE} \cdot I^2 + \frac{2\sqrt{2}}{\pi} V_{CES} \cdot I \right]
\end{aligned} \tag{5.13}$$

where N_c is the cascade number, indicating the number of modules connected in series in each phase. The filter contains an inductance, which also has a parasitic resistance. Other losses, such as the iron and eddy current losses in the core, are neglected for simplicity. The power consumed by the filter is therefore given by

$$P_{filter} = R \cdot I^2 \tag{5.14}$$

Switching losses

In the event-based model, the switch transitions occur instantly, and induce a power loss according to the voltage and current at that given time. The dependency is given by equation 4.16. As explained later, for all non-negligible switching events, the voltage is constant and equal to the battery module voltage V_{DC}. Time-averaging 4.16 over one period of the current gives an expression for the average energy loss. For example, for the turn-on energy this gives

$$\begin{aligned}
\langle E_{on} \rangle &= \frac{1}{T} \int_0^T \frac{V}{V_{ref}} \left[a_{on} \cdot i^2(t) + b_{on} \cdot |i(t)| + c_{on} \right] \, dt \\
&= \frac{1}{T} \int_0^T \frac{V}{V_{ref}} \left[a_{on} \cdot i^2(t) + b_{on} \cdot |i(t)| + c_{on} \right] \, dt \\
&= \frac{2}{T} \int_0^{\frac{T}{2}} \frac{V}{V_{ref}} \left[a_{on} \cdot \hat{I}^2 \sin^2(\omega t) + b_{on} \cdot \hat{I} \sin(\omega t) + c_{on} \right] \, dt \\
\Rightarrow \langle E_{on} \rangle &= \frac{V}{V_{ref}} \left[a_{on} \cdot I^2 + \frac{2\sqrt{2}}{\pi} b_{on} \cdot I + c_{on} \right]
\end{aligned} \tag{5.15}$$

As indicated by Table 4.1, 12 switching events occur per switching period. The diode turn-on event is negligible in power loss compared to the turn-off. Furthermore, when the current switches between two devices connected in parallel (IGBTs and diode), the voltage stays nearly zero. This means that according to equation (4.16), the incurred loss is nearly zero as well. Ingoring these two type of events, leaves only 6 significant switching events per period. These events are evenly divided across the three categories: 2 IGBT turn-on events, 2 IGBT turn-off events and 2 diode turn-off events. These time-averaged values are then multiplied with the number of times they occur during a period of the current

$$\begin{aligned}
\langle P_{sw} \rangle &= f_{sw} \cdot 3N_c \cdot [2\langle E_{on} \rangle + 2\langle E_{off} \rangle + 2\langle E_{rec} \rangle] \\
&= 6N_c f_{sw} \frac{V_{DC}}{V_{ref}} \left[a_t \cdot I^2 + \frac{2\sqrt{2}}{\pi} b_t \cdot I + c_t \right]
\end{aligned} \tag{5.16}$$

where

$$\begin{aligned}
a_t &= a_{on} + a_{off} + a_{rec} \\
b_t &= b_{on} + b_{off} + b_{rec} \\
c_t &= c_{on} + c_{off} + c_{rec}
\end{aligned} \tag{5.17}$$

Impact of N_c

Overall, the cascade number N_c increases the power losses. The same amount of current has to go through a higher number of switching devices, which increases the conduction losses.

The switching losses are not affected; this is because the losses scale with the battery module voltage. To make the comparison fair, the total amount of voltage remains the same

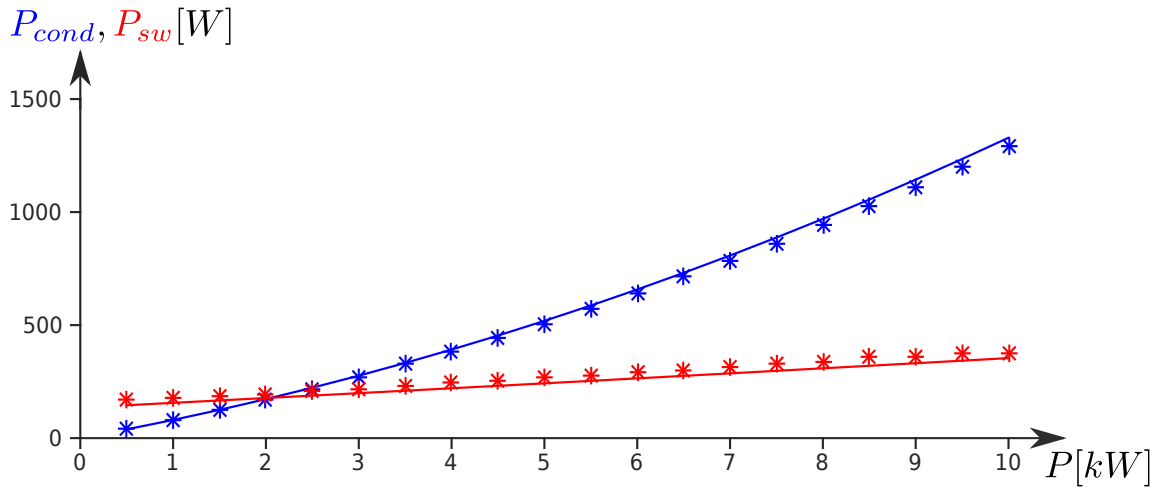
$$N_c' \dot{V}_{DC}' = N_c \dot{V}_{DC} = V_{DC,total} \tag{5.18}$$

This is also achievable in reality for a given system, because battery modules often consist of several smaller modules. By removing modules from all existing units, a new unit is created. Since the number of modules in use stays the same, so does the total available voltage. Then, according to equation (5.16), the switching losses remain unaffected.

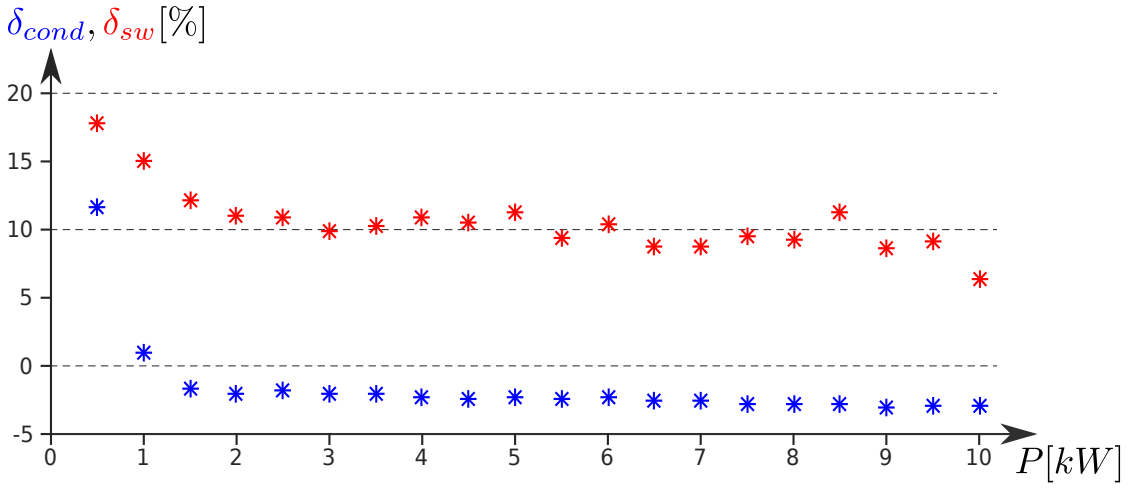
5.3.2 Simulation results

Fig. 5.6 shows are comparison of the simulation results and the predictions of the analytic formulas. Overall the formulas offer a good approximation, reaching an accuracy of around 5% at nominal power.

There are two differences between the formulas and the simulation. First and foremost, the formulas neglect the harmonics in the steady-state current. When the power output increases, the fundamental component of the current increases; the harmonics stay the same. Therefore, the relative share of the harmonics in the current becomes less significant. This also reduces the relative error in the analytic formulas. Fig. 5.6b clearly demonstrates this. As the power output goes to zero, the relative error becomes larger and larger. Secondly, the analytic formula makes a continuous approximation of the discrete switching events. This also causes a deviation between the formula and the simulation results.



(a) The switching and conduction losses increase with the load. The dots show the simulation results, whilst the full line indicates the prediction of the analytic formulas.



(b) Relative error

Figure 5.6: The analytic formulas offer a good approximation, especially at higher load. The harmonics are not included in the analytic formulas, and are the main cause of the difference with the simulation results. The harmonics don't change with the load. At higher load, the harmonic are less significant compared to the fundamental, and the approximation improves.

5.3.3 Efficiency

The efficiency of the converter is the ratio of the output power to the input power. The difference between both is the power loss

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{loss}}{P_{in}} = 1 - \frac{P_{loss}}{P_{in}} \tag{5.19}$$

For highly efficient systems, the efficiency is approximately equal to

$$\eta \approx 1 - \frac{P_{loss}}{P_{out}} \tag{5.20}$$

What the input and output is, depends on whether the converter is charging or discharging. For example, when the batteries are charging, power flows from the batteries, through the converter, to the grid. Time-averaged values of the power flows are used. This means that only the fundamental current has an impact on the output power; the harmonics produce no average power flow when connected to an ideal voltage source. The efficiency is then equal to

$$\eta = 1 - \frac{P_{cond} + P_{sw} + 3P_{filter}}{3VI} \tag{5.21}$$

Using the analytic formulas, the loss components can be expressed as a function of the current. This leads to

$$\eta = 1 - \left(A \cdot I + B + C \cdot \frac{1}{I}\right) \tag{5.22}$$

where A,B and C represent compactly a product of several parameters. This clearly shows the current dependency. When the current and hence the output power is close to zero, the C-term dominates. As the current increases, the efficiency increases as the C-term decreases. This term is due to fixed component of the switching losses. As the current increases further, the A-term starts to dominate. The efficiency reaches a maximum, where after the disproportional increase of the quadratic components leads to a decrease in efficiency. As Fig. 5.6a shows, mostly the conduction losses contribute to the quadratic components.

Fig. 5.7 shows the efficiency as predicted by the analytic formulas, and the results of the simulation. The simulated efficiency is lower and reaches its maximum later. This is due to the presence of harmonics in the simulation. The harmonics induce additional switching and conduction losses. These losses behave roughly as a C-term.

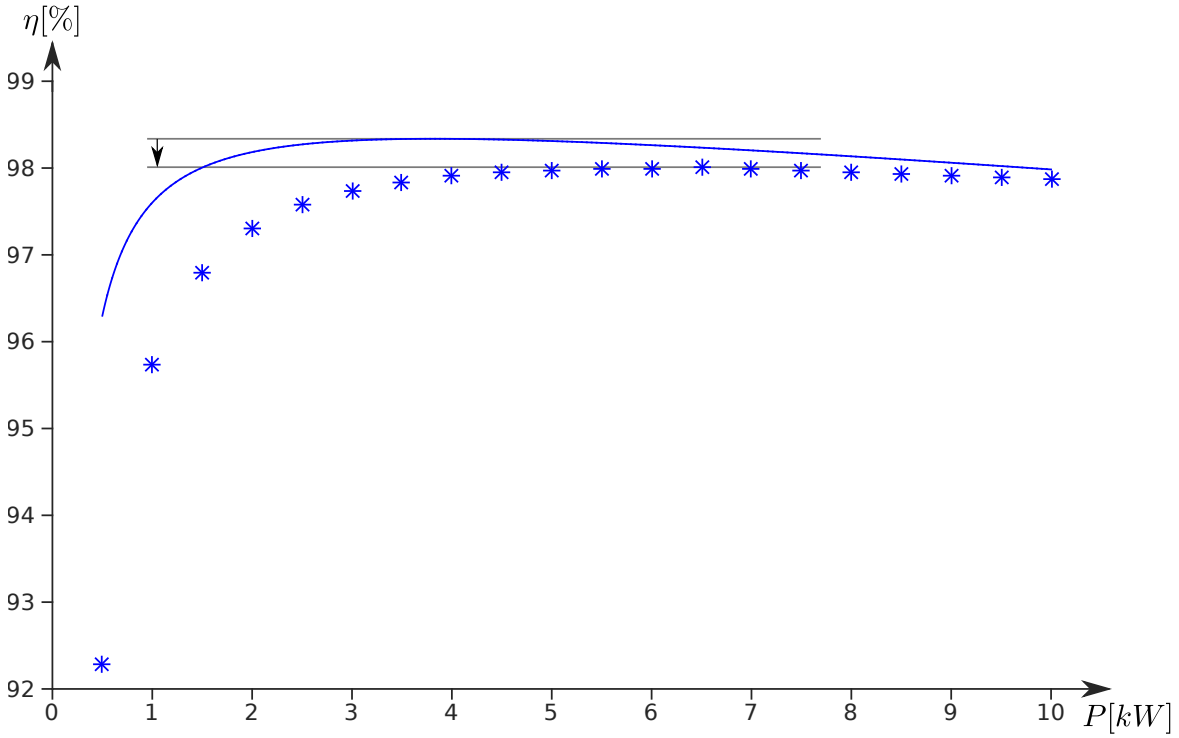


Figure 5.7: The efficiency of the simulation (dots) is lower than the efficiency predicted by the formulas (line). The extra switching and conduction losses due to harmonics are not included in the formulas, and are especially significant at low power output.

This discrepancy between simulation and formulas therefore diminishes as the power output increases.

5.4 Power quality

5.4.1 Fourier analysis

Analyzing the waveforms in the frequency spectrum leads to several key insights and deeper understanding of the converter. In general, the Fourier transformation can transform almost any signal from the time domain to the frequency domain.

After the initial transient caused by the change in set point, the current controller quickly moves the converter to steady-state. In steady-state, the waveforms are periodic. All electrical variables repeat periodically with the grid frequency, f_n. In steady-state, the frequency spectrum is discretized; only multiples of f_n are present. If this was not the case, the waveform would not be periodic.

For periodic signals, the general Fourier transform reduces to the Fourier series decomposition. There are a few equivalent definitions of the Fourier series decomposition. The most useful one for this application is

$$x_P(t) = \frac{\hat{X}_0}{2} + \sum_{i=0}^{\infty} \hat{X}_i \sin\left(i \cdot w_n t + \phi_i\right) \tag{5.23}$$

From this definition, it is immediately clear that the periodic signal x_P is decomposed into a series of sines at multiples of the grid frequency, each with a unique amplitude and phase shift. These higher frequency components can be represented by a phasor, with the rms value X_i as its amplitude [46].

The component of the series at the grid frequency is called the fundamental component. All components at a higher frequency are the harmonic components, or shortly, harmonics. Harmonics are undesirable as they cause losses and disturbances [47]. The objective of this section is to analyze the harmonics present in the current injected into the grid.

In this context, the total harmonic distortion (THD) is a metric indicating the presence of harmonics. This metric is useful to compactly display information about the harmonic content. The THD is given by

$$THD = \frac{\sqrt{\sum_{i=2}^{\infty} X_i}}{X_1} \tag{5.24}$$

$$= \frac{\sqrt{X_{RMS}^2 - X_1^2}}{X_1} \tag{5.25}$$

[46].The first equation shows the idea behind the metric: a Euclidean norm on all harmonic components, compared to the fundamental component. The second equation is equivalent but more useful in practical calculations. The equivalence follows from the fact that all components of the Fourier series are orthogonal functions and by assuming that there is no DC-component.

5.4.2 Regulation and standards

Harmonics have a wide range of negative effects, reducing the power quality of the system. They induce losses in motors, generators and capacitors and lead to misoperation in electronics, switchgear and relaying [47]. Because of the diverse range of negative effects, it is hard to specify which harmonics are more harmful than others. Standard IEEE Std 519-1992 provides a reference point to assess exactly this.

The Institute of Electrical and Electronics Engineers (IEEE) released a standard with best practices to deal with harmonics, referred to as IEEE Std 519-1992. This was motivated by the increased popularity of non-linear loads. Many devices include power converters, which provide many benefits: energy savings, improved process control, higher reliability... But the big drawback is that they turn the devices into non-linear loads from the system perspective, generating harmonics. [48]

There are two main parties: the user and the system operator. The user connects to the system at the point of common coupling (PCC). The standard assigns responsibilities to both parties. It is the duty of the system operator to maintain a clean voltage at the PCC. But at the same time, the consumer has to inject a clean current into the system. [47] What makes a current waveform clean or not, is exactly the subject of the remainder of this section. A harmonic emission norm specifically for generators, is given by IEC61000-4-15.

The voltage generated by the converter leads to a current injection into the source. IEEE Std 519-1992 defines upper limits for the harmonics present in the injected current. There are two types of restrictions. A first type of restriction defines a limit of each harmonic separately, with lower limits for higher order harmonics. A second type of restriction is defined in terms of total demand distortion (TDD), a metric similar to the THD.

Table 5.2 gives an oversight of these limits. Different limits apply depending on the ratio of the maximum load current I_L to the short-circuit current I_{SC}. Higher harmonics are tolerated for a higher I_L and a lower I_{SC}. The limits on the individual harmonics

Table 5.2: IEEE Std 519-1992 specifies limits for harmonics, shown in percentage, relative to the maximum load current. In addition, it specifies a limit for the total THD of the current. This table specifies the limits for odd harmonics. For the even harmonics, stronger restrictions are in place: only 25% of the odd ones. I_{SC}/I_L is the ratio of short-circuit current to the maximum demand load current. [47]

Odd harmonic limits $lim_h\left(I_{SC}/I_L\right), h = 2k+1$						
$\frac{I_{SC}}{I_L}/h$	<11	11-17	17-23	23-35	>35	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

are defined as a fraction of the I_L. Table 5.2 only lists the limits for odd harmonics; the limits for even harmonics are 75% lower. The TDD only differs from the THD in having the maximum load current in its denominator instead of the fundamental component. When the converter is operating at maximum load, the maximum load current is equal to the fundamental component of the current by definition. In this case, TDD and THD are the same.

The usefulness of these restrictions are not undisputed. Barr and Gosbell suggest instead to use only four restrictions, instead of the more than 40 imposed by IEEE Std 519-1992. They define some new metrics based on weighted averages of harmonics, and impose restrictions only on these averages. They argue that these new metrics more accurately reflect the impact on critical physical effects. [49] This thesis observes these remarks, but will stick to the limitations established by IEEE Std 519-1992. [49]

5.4.3 Analysis of base case

The limits imposed by IEEE Std 519-1992 depend on the ratio of the maximum load current I_L to the short-circuit current I_{SC}. I_L is simply equal to I_{AC}, the current rating (5.2). I_{SC} on the other hand depends on the grid to which the converter is connected. This thesis will compare the converter performance to the most strict restrictions of IEEE Std 519-1992. The alternative is choosing a specific grid which might lead to less strict limits, but will also render the analysis less general.

Fig. 5.8 shows the current waveform for the base case. The blue curve represents the fundamental component, whilst the red line indicates the ripple current, the cumulative result of all harmonic components.

Fig. 5.9 shows the harmonic components of the ripple current in percentage of the

fundamental component. The even and odd components are shown in separate figures, because different limits apply. The even harmonics are significantly lower than the odd ones. Fig. 4.10 in subsection 4.2.2, shows an ideal waveform generated by a single cluster. The first half of the waveform is the opposite of the second half, meaning it is an odd funcion. Odd functions only have odd harmonic components in their Fourier decomposition. This explains the dominance of the odd components. In reality, due to ripple in the reference signal and other imperfections, there will be a limited amount of even components.

The dominant odd harmonic components are centered around the 120th harmonic

$$f'_{sw}(N_c = 3) = 2f_{sc} \cdot 3 = 120f_p \tag{5.26}$$

This is the combined result of the U-PWM at the cell level, and the sub-harmonic method at the cluster level. The U-PWM halves the period of the switching waveform, while the sub-harmonic method lowers it further by the number of cells, the cascade number N_c. This results in a signficantly higher effective switching frequency f'_{sw}. A very important design consideration related to this is discussed in 5.4.4.

Fig. 5.9 shows the limit set by IEEE Std 519-1992 for each harmonic with a green line. harmonic components which exceed this limit, are colored in red. The converter with 3 levels and the initial inductance sizing, does not respect the limits. The dominant harmonic components centered around the effective switching frequency, are more than 7 times in excess of the limit. The next subsection will discuss how to solve this, and make the converter IEEE Std 519-1992 compliant.

5.4.4 Variation under key parameters

The 3-level converter with the initial inductance sizing does not comply with IEEE Std 519-1992. This subsection will examine the impact of two parameters on the harmonic performance: the cascade number N_c and the inductance L. By increasing one or both parameters in the correct way, the converter will comply with the standard.

Equation (4.1) describes the dynamics of the voltages and current in each phase. Transforming it to the frequency domain, gives

$$V_{Cu}(f) - V_{Su}(f) = (L2\pi f + R)\, I_u(f) \tag{5.27}$$

V_{Su} is the grid voltage, and is assumed to be harmonics free. Therefore, it only has a

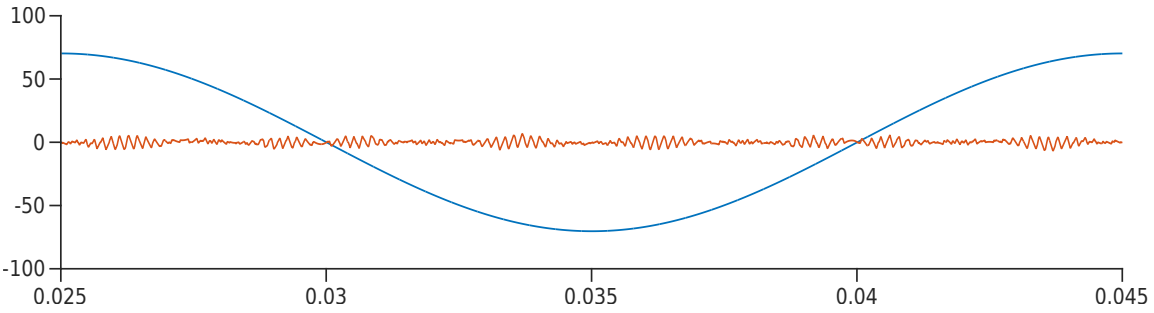
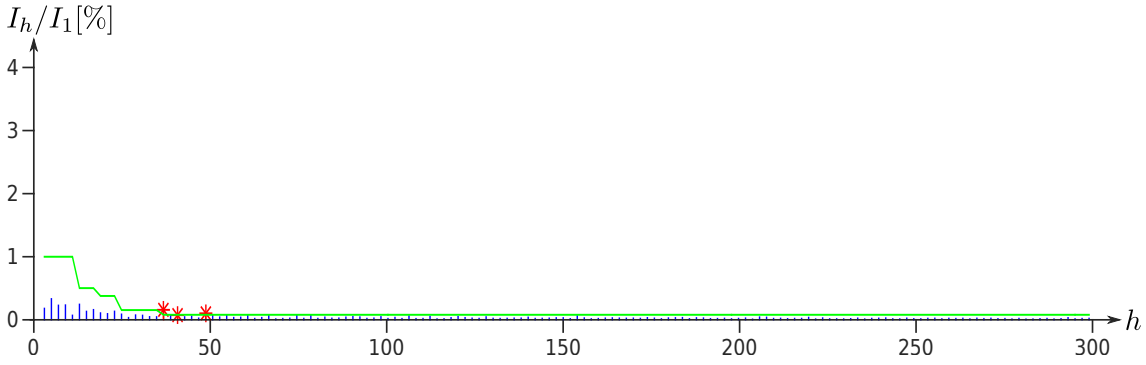
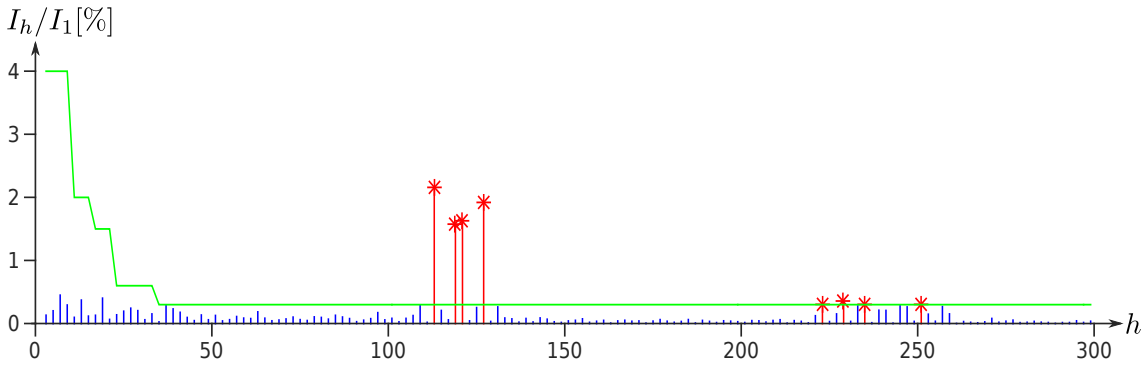


Figure 5.8: The harmonics cause a ripple in the current waveform in the time domain. The blue curve shows the fundamental component, whilst the red curve shows the combination of all harmonic components in the time domain.



(a) Even harmonics



(b) Odd harmonics

Figure 5.9: The green line indicates the limits set by IEEE Std 519-1992, corresponding with Table 5.2. The harmonic components exceeding the limit are shown in red.

fundamental component

$$V_{Su}(f) = 0 \qquad if \quad f \neq \omega_n \tag{5.28}$$

For all other frequencies, this means that the harmonic current only depends on the harmonic converter voltage at the same frequency. If the frequency is larger than the cutoff-frequency f_c, this leads to a simple transfer function

$$\begin{aligned} |H(f,L)| &= \left| \frac{1/R}{1 + j2\pi f \frac{L}{R}} \right| \qquad f \gg f_c = \frac{R}{2\pi L} \\ &\approx \frac{1}{2\pi} \frac{1}{L} \frac{1}{f} \end{aligned} \tag{5.29}$$

The damping of the harmonic components is proportional to the frequency and the inductance.

Inductance

Fig. 5.10a shows the harmonic components which exceed their limits. The components are further normalized with respect to the limit, and will be referred to as $I_r(h)$

$$I_r(h) = \frac{I_h/I_1}{lim_h} \tag{5.30}$$

For example, a value of 1 means that the harmonic component exactly matches the limit. Applying equation (5.29) leads to an expression for $I_r(h)$ in terms of the inductance

$$I_r(h) = \frac{lim_h}{I_1} V_h H(hf_p) = \frac{lim_h V_h}{2\pi(hf_p)I_1} \frac{1}{L} \tag{5.31}$$

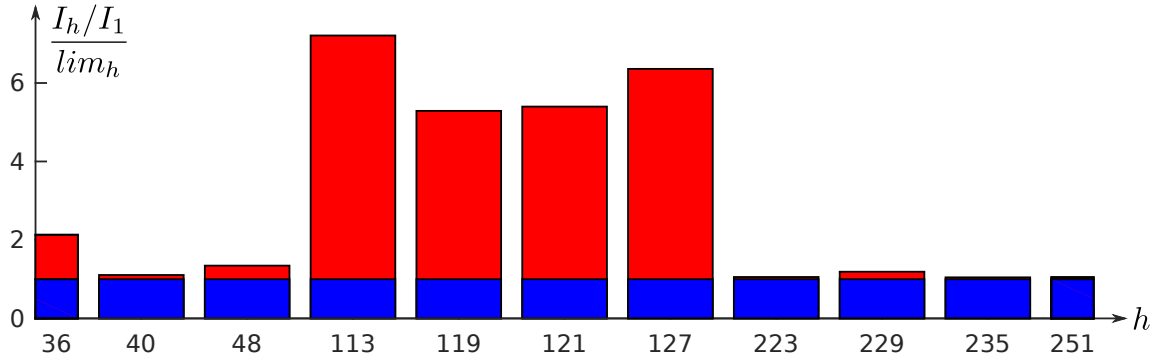
Increasing the inductance to L' will lower the harmonic current to I'_r

$$\frac{L'}{L} = \frac{I_r(h)}{I'_r(h)} \tag{5.32}$$

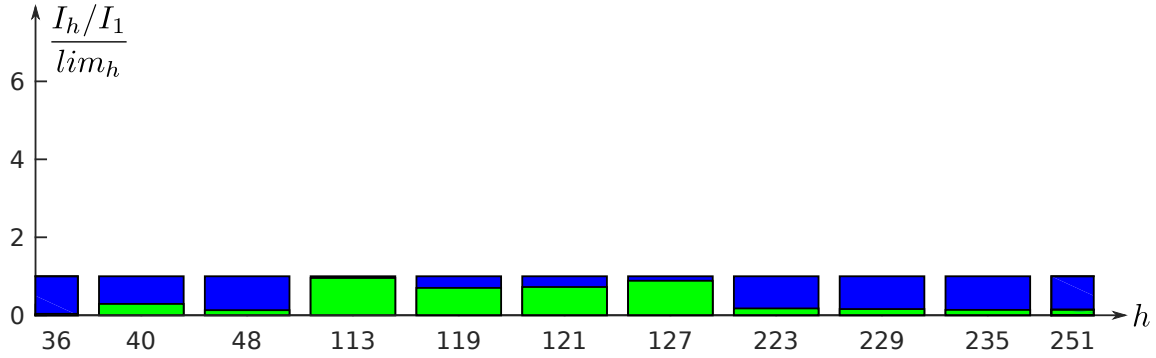
This leads to a simple design rule. Select the largest harmonic component $I_r(h)$ and increase the inductance until it meets the limit (hence $I'_r = 1$)

$$\frac{L'}{L} = \max_h \left[I_r(h) \right] \tag{5.33}$$

This will ensure that all other components are below their limits as well, because they scale in the same way. Fig. 5.10 shows the result of this method for the base case. The normalized harmonic components in Fig. 5.10b are all below the limit. Harmonic component 113 was the biggest. The inductance was increased so that this harmonic would exactly meet the limit. All others also meet their limit as a consequence. Note that the suggested value of $10.1mH$ ($7.21L$) also respects the requirement for the short-circuit impedance (5.5).



(a) Before inductance tuning



(b) After inductance tuning with $L' = 7.21L$

Figure 5.10: The harmonics in percent of the fundamental are normalized relative to the limit valid at each harmonic. The blue bar indicates the value 1, when the harmonic matches exactly the limit. The new inductance size guarantees that all limits are met.

Cascade number

The cascade number impacts the harmonics. It does not affect the filter, but it changes the input to the filter: the harmonics present in the converter voltage. First, the details of the modulation technique are briefly reviewed. This reveals the impact of the cascade number on the harmonics.

The modulation takes place on two levels: cell level and cluster level. On the cell level, the individual switches are coordinated in order to get a specific output waveform at the cell terminals. U-PWM modulation the harmonic performance of the individual cell. By creating a waveform which repeats twice in one switching period, the effective switching frequency is doubled. There are two inputs to this process: the reference and the phase of the trigger. The cluster level coordinates the cells in a single cluster, which are connected in series. The sub-harmonic method shifts the phases of the triggers of the individual cells by $\frac{360°}{N_c}$. This also improves the switching frequency, because the cluster voltage repeats N_c times in one switching period.

On both levels, the waveform is repeated in a single switching period, 2 and N_c times. Do these two effects combine to $2N_c$ repetitions? It depends on N_c. If N_c is even, then the first $\frac{N_c}{2}$ repetitions will coincide with the second half. Therefore, the total amount of repetitions is only N_c. If N_c is odd, this does not happen. The effective switching frequency is equal to the switching frequency multiplied by the number of repetitions in a switching period

$$f'_{sw} = \begin{cases} 2 \cdot N_c \cdot f_{sw} & N_c \text{ is odd} \\ N_c \cdot f_{sw} & N_c \text{ is even} \end{cases} \tag{5.34}$$

Fig. 5.11 shows the odd harmonics for a converter with N_c varying from 3 to 7. The cummulative voltage of all batteries together is kept constant. Therefore, the voltage of each individual battery module is scaled down as the number of batteries increases. New battery modules contain several sub-units, so this could also be achieved in reality.

The dominant harmonics occur around the effective switching frequency. As N_c increases, f'_{sw} increases. Centered at the higher frequency, the dominant harmonics are filtered more; the damping is proportional to the frequency. A higher N_c generally improves the harmonic performance. But note that the converter with even N_c performs significantly worse than with odd N_c. It requires an even N_c of 6 to match the performance of an even N_c of 3. This leads to a simple design rule: make sure N_c is odd. Raising N_c to 7 is sufficient to lower all harmonics below the limits.

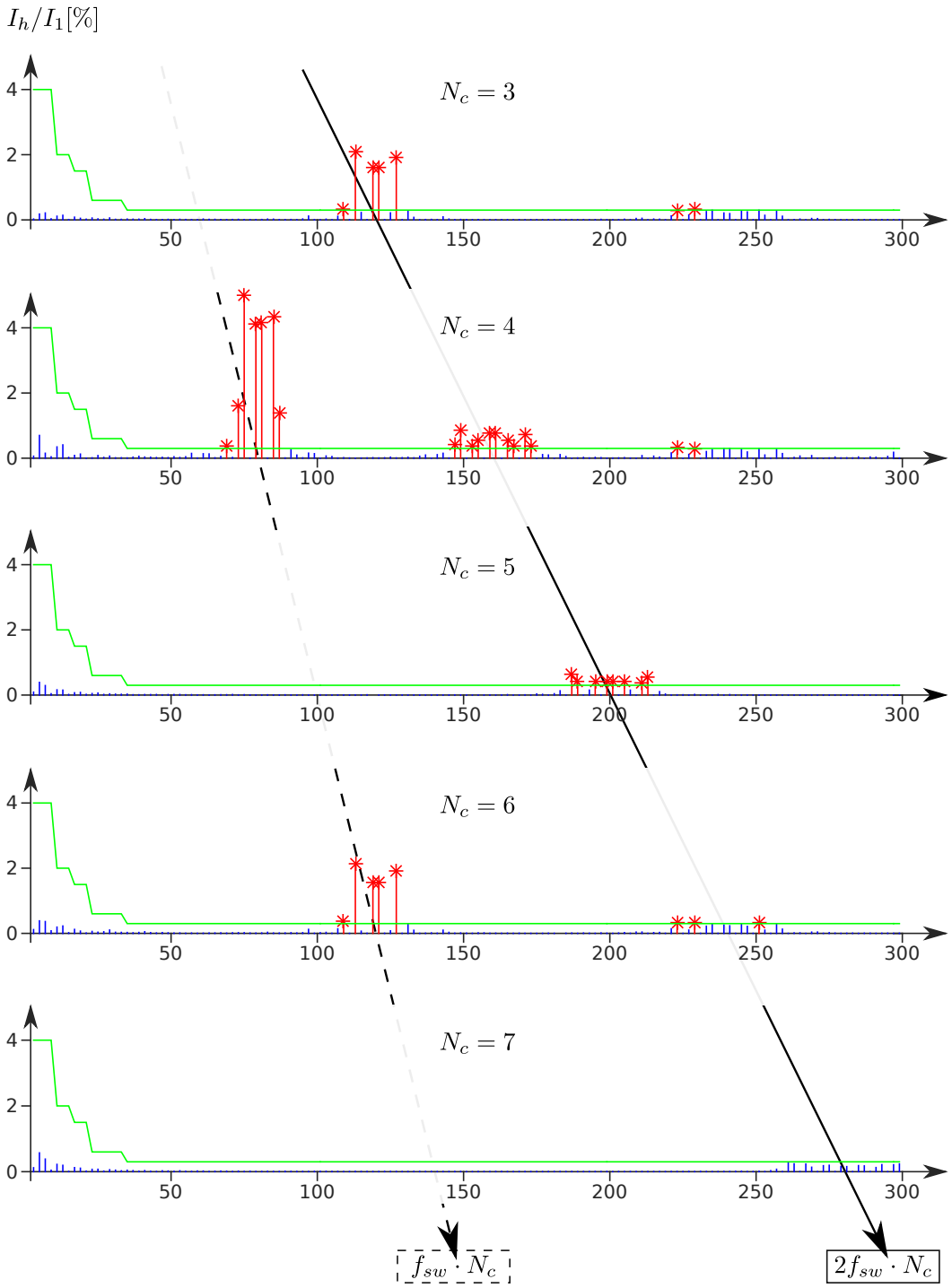


Figure 5.11: The odd harmonics change with the number of cells N_c. The cummulative voltage of all batteries together is kept constant; all other parameters of the design stay unchanged. Increasing N_c shifts the effective switching frequency to the right according to equation (5.34). Higher frequencies are filtered more, so the harmonic performance increases. Note that an even N_c leads to a significantly worse performance. At $N_c = 7$, all harmonics are lowered below the allowed limits.

5.5 Reliability

Most modern inverter designs are based on multilevel topologies. These designs improve the power quality by combining multiple small voltage steps. Additionally, this results in lower losses and improved electromagnetic current. There is one big drawback: the increased number of switches [45]. For the SSBC-MMCC converter, the number of switches is $12N_c$. For example, a simple three-level inverter has 36 switches. This is already 6 times more than a classical six-pulse inverter.

This leads to concerns regarding the reliability. The likelihood that a single switch fails increases as the total number of switches increases. This is especially troubling in applications where shutting the converter is very costly or even dangerous; downtime in industrial processes and Navy propulsion systems are such applications [45]. Therefore, several authors address this concern by developing techniques allowing the converter to continue operating, even when a fault occurs. [16, 25–28, 50]

This thesis will adopt a mechanism similar to the one proposed by Lezana et al. [27] and Rodriquez et al. [26]. When a cell becomes faulty, the control system bypasses the cell. To compensate for this loss, the control system adjusts the phase shift of the trigger and the reference voltage of the remaining cells. The first subsection derives the changes required by this mechanism. The second subsection will simulate a battery short-circuit to demonstrate this mechanism.

5.5.1 Requirements for continued operation

When a battery module becomes unavailable, the other battery modules can compensate and keep the converter operational. There might be several causes for this: a short-circuit in the bridge cell, taking the battery offline for maintenance etc. Temporarily running the converter with one battery module less offers more flexibility and reliability. This subsection will examine what the requirements are for this to be possible.

V_{DC} is the available voltage for the modulation of an entire cluster, the sum of the voltages of all battery modules in that cluster. The average output voltage of the cluster depends on the modulation, and ranges from $-V_{DC}$ to V_{DC}. The minimum requirement is

$$V_{DC} > \sqrt{2}V_{AC} \tag{5.35}$$

This guarantees that the converter can achieve the peak of the AC voltage of the grid it is connected to, and dictates a lower limit for the amount of connected battery cells for a given V_{AC}. Therefore, extra battery cells are added, so that when a module goes offline, enough battery cells remain to meet this minimum V_{DC}. There is no physical distinction between normal and backup cells; all cells participate equally in the modulation. These extra cells are even useful: though not necessary to meet the minimal operation requirements, they increase the energy storage capacity of the BESS.

The modulation index is the ratio between V_{DC} and the maximum value of the reference signal

$$m_a = \frac{\hat{v}_{ref}}{V_{DC}} \tag{5.36}$$

When a battery becomes unavailable, the remaining batteries have to increase their share of the total required voltage. They can only compensate for the unavailable battery if the modulation index before was low enough

$$\begin{aligned} & \sqrt{2}V_{AC} < m'_a V_{DC}\,(N_c - 1) \\ \Leftrightarrow \quad & \sqrt{2}\frac{m_a V_{DC} N_c}{\sqrt{2}} < m'_a V_{DC}\,(N_c - 1) \\ \Leftrightarrow \quad & m_a < m'_a \frac{N_c - 1}{N_c} \end{aligned} \tag{5.37}$$

The modulation index was only 90% in the base case. This margin of 10% prevents saturation during steady-state. The ripple present in the current, enters the feedback loop and causes some ripple in the reference voltage. If m_a was exactly one, the reference voltage would repeatedly saturate when the reference voltage nears its peak.

In order to guarantee that m'_a is still 90% in the base case, m_a should be lower than

$$m_a < 90\% \frac{3-1}{3} = 60\% \tag{5.38}$$

if the cascade number N_c remains unchanged. This can be achieved by increasing the initial available V_{DC} to

$$V'_{DC} = V_{DC} \frac{N_c}{N_c - 1} = 350V \frac{3}{2} = 525V \tag{5.39}$$

5.5.2 Simulation of a battery short-circuit

To demonstrate the potential of this mechanism, a battery fault and subsequent control is simulated. At $t = 0.04s$, a short-circuit occurs in the first bridge cell. The battery management system (BMS) detects an unusual power drain and disconnects the battery. The modulation control is connected to the BMS of each battery, and is notified of the unavailability of the first battery module. Therefore, it switches to two level operation by adjusting the phase shift and reference voltage of the two remaining battery modules.

Fig. 5.12 shows the waveforms of the converter for the u-phase, before and after the fault occurs. Initially, N_c is odd. When battery module 1 goes offline, N_c becomes even. This has a very negative impact on the harmonic performance, causing a significantly bigger ripple in the current. It could be better to further reduce the N_c post-fault to an odd number. In this specific case that wouldn't impact the harmonics, because $N_c = 1$ and $N_c = 2$ lead to the same harmonic performance. But if N_c was initially 7, removing two levels would lead to a much smoother current waveform (see Fig. 5.11). The downside of this is that the batteries will have to be oversized even further.

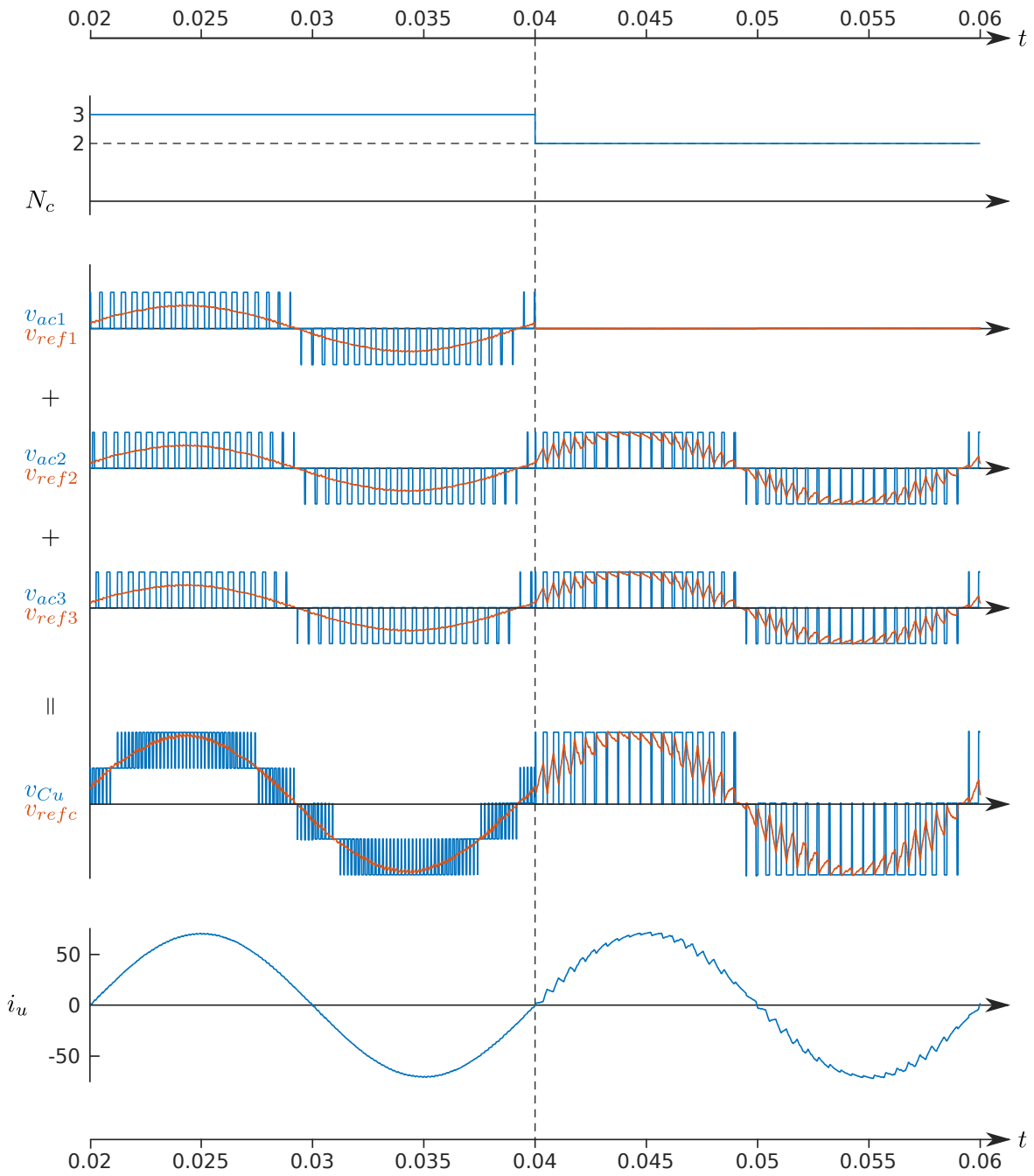


Figure 5.12: At $t = 0.04$, battery module 1 goes offline. The cascade number N_c reduces from 3 to 2. The modulation control automatically adjusts the phase shift and the reference voltage of the other battery modules. The converter voltage is maintained. Note that the $N_c = 2$ operation has a larger ripple current. The ripple current also enters the feedback loop, and causes a ripple in the reference voltage.

Chapter 6

Conclusion

The main objective of the thesis is to develop a tool which simulates the behavior of a MMCC-SSBC converter. As a secondary objective, the thesis strives to demonstrate the usefulness of this tool. This chapter will discuss how this twofold objective was achieved, and will give suggestions for further research.

The main objective is fulfilled by the core deliverable of the thesis: a Matlab implementation of a dynamic model of the converter. Appendices B and C provide a detailed description of the core deliverable. Chapter 4 describes the theoretical underpinning of this implementation. The model consists of three layers: interface and control, converter operation and loss model. For each of these layers, a specific implementation has been developed; both a conceptual description and a Simulink implementation. The Matlab implementation together with the documentation provided by Chapter 4, fulfill the main objective.

The thesis also aims to demonstrate the usefulness of the developed tool. This is achieved primarily by the case study described in Chapter 5. The case study chooses specific ratings for a typical converter. With the help of the tool, three key characteristics are discussed: efficiency, power quality and reliability. This leads to some important insights, which will be briefly summarized. Analyzing the power quality led to two simple design rules. Firstly, the cascade number N_c should be uneven. Secondly, the inductive filter can be scaled according to a simple rule in order to comply with a harmonic emission standard. The efficiency is negatively impacted by harmonic current, even more so for lower load levels. Finally, the thesis demonstrates that the converter can keep on operating when a battery module fails. The tool helped significantly in arriving at and validating these conclusions.

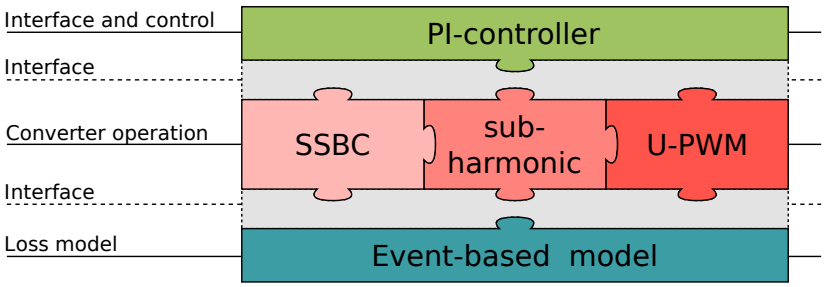
Secondarily, the tool is useful due to its layered structure. Each layer's implemen-

tation can be changed independently. Fig. 6.1a demonstrates this principle. The layers communicate through an interface. As long as a new layer implementation respects the interface connection, the model as a whole remains functional. This allows the user to quickly prototype a new method. For example, assume the user wants to study a phase-disposition modulation method instead. The user only has to change the implementation of the converter operation layer; the other layers remain unaffected.

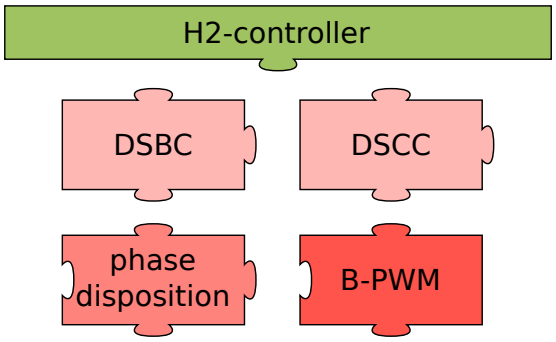
The most critical step for further research is model validation. Due to practical restrictions, it was not possible to build an experimental setup of the SSBC-MMCC converter. The model has only been validated by comparing it to an online simulation tool provided by a semiconductor manufacturer. There was no extensive documentation available for this tool, so it could only be verified that the losses were of a similar magnitude. Therefore, the next step should be a thorough model validation in order to justify any conclusions based on it.

Once the model has been validated, there are two main pathways for further research. Firstly, the researcher could further expand on the case study. For example, the cost of the proposed solution has not been considered. Secondly, the layered model provides an excellent basis for comparison studies. Fig. 6.1a illustrates this approach and shows some alternatives. The researcher can easily change a part of the implementation. The tool remains functional under this change. The researcher can then compare the old and new implementation. For example, the researcher could try out a different modulation technique and compare the resulting harmonics. This approach offers a lot of research opportunities. Finally, this thesis modeled the batteries as ideal voltage sources. Further research should extend the model with a realistic battery model, especially when SoC balancing is considered.

The thesis fulfilled its main objective. Additionally, the thesis demonstrated the usefulness of the tool in two ways: by applying it to a case study and by pointing out further research based on it. Hopefully, it proves to be instrumental in showing the potential of this topology, and in promoting its adoption in the industry.



(a) Implementation of layers



(b) Some alternative implementations

Figure 6.1: One pathway for further research is comparing several alternative implementations, and how they affect the converter performance.

Chapter 7

Acknowledgement

To conclude, I would like to thank the institutions and persons who enabled the creation of this thesis. Firstly, there is the Smart Cities master programme, a collaborative effort between 4 European universities. They allowed me to study abroad at both the Royal Institute of Technology in Stockholm and at the Universitat Politècnica de Catalunya. Furthermore, they provided financial support through KIC InnoEnergy throughout the studies. Secondly, I would like to thank Dr. Gonzalez who supervised the creation of this thesis. He provided guidance when the path forward was unclear, and feedback when I thought the path was clear. I doubt I will ever meet his equal when it comes to answering emails quickly. Finally, I would like to thank Konstantinos Spiliotis. He proofread parts of this thesis as I wrote them. Also, he gave me the chance to collaborate with him on a paper which we presented at the European Energy Market 2016 conference. The experience I gained writing this paper, was very helpful when I wrote this thesis.

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Appendix A

Datasheets

A.1 IGBT module FS100R17KE3

IGBT,Wechselrichter / IGBT,Inverter

Vorläufige Daten
Preliminary Data

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C	V_{CES}	1700	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 80°C, $T_{vj\,max}$ = 150°C T_C = 25°C, $T_{vj\,max}$ = 150°C	$I_{C\,nom}$ I_C	100 145	A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	200	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 150	P_{tot}	555	W
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 100 A, V_{GE} = 15 V I_C = 100 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C	$V_{CE\,sat}$		2,00 2,40	2,45	V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 4,00 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	5,2	5,8	6,4	V
Gateladung Gate charge	V_{GE} = -15 V ... +15 V		Q_G		1,20		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C		R_{Gint}		7,5		Ω
Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		9,00		nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		0,29		nF
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 1700 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			5,0	mA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 100 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Gon} = 4,0 Ω	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,on}$		0,37 0,40		µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 100 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Gon} = 4,0 Ω	T_{vj} = 25°C T_{vj} = 125°C	t_r		0,04 0,05		µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 100 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Goff} = 4,0 Ω	T_{vj} = 25°C T_{vj} = 125°C	$t_{d\,off}$		0,65 0,80		µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 100 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Goff} = 4,0 Ω	T_{vj} = 25°C T_{vj} = 125°C	t_f		0,18 0,30		µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 100 A, V_{CE} = 900 V, L_S = 30 nH V_{GE} = ±15 V R_{Gon} = 4,0 Ω	T_{vj} = 25°C T_{vj} = 125°C	E_{on}		22,0 32,0		mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 100 A, V_{CE} = 900 V, L_S = 30 nH V_{GE} = ±15 V R_{Goff} = 4,0 Ω	T_{vj} = 25°C T_{vj} = 125°C	E_{off}		21,5 31,5		mJ mJ
Kurzschlußverhalten SC data	$V_{GE} \leq$ 15 V, V_{CC} = 1000 V $V_{CEmax} = V_{CES} - L_{sCE} \cdot di/dt$	$t_P \leq$ 10 µs, T_{vj} = 125°C	I_{SC}		400		A
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			0,225	K/W
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		125	°C

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Vorläufige Daten
Preliminary Data

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	1700		V
Dauergleichstrom Continuous DC forward current		I_F	100		A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	200		A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	1800		A²s

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 100 A, V_{GE} = 0 V I_F = 100 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C	V_F		1,80 1,90	2,20	V V
Rückstromspitze Peak reverse recovery current	I_F = 100 A, - di_F/dt = 2450 A/µs (T_{vj}=125°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	I_{RM}		155 165		A A
Sperrverzögerungsladung Recovered charge	I_F = 100 A, - di_F/dt = 2450 A/µs (T_{vj}=125°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	Q_r		29,0 48,5		µC µC
Abschaltenergie pro Puls Reverse recovery energy	I_F = 100 A, - di_F/dt = 2450 A/µs (T_{vj}=125°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C	E_{rec}		15,5 27,5		mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			0,39	K/W
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		125	°C

NTC-Widerstand / NTC-Thermistor

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Nennwiderstand Rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R100 Deviation of R100	T_C = 100°C, R_{100} = 493 Ω	ΔR/R	-5		5	%
Verlustleistung Power dissipation	T_C = 25°C	P_{25}			20,0	mW
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/50}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/80}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/80}$		t.b.d.		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/100}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/100}$		t.b.d.		K

Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

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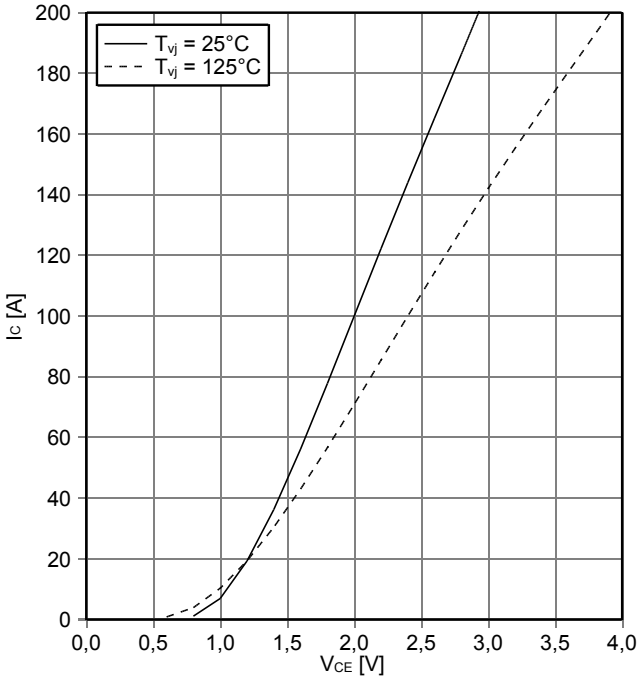
Vorläufige Daten
Preliminary Data

Modul / Module

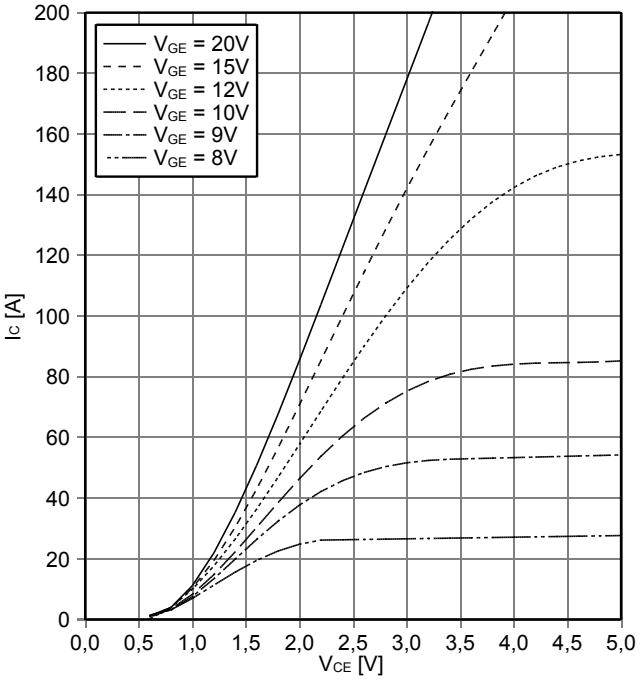
Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		3,4		kV
Material Modulgrundplatte Material of module baseplate				Cu		
Innere Isolation Internal isolation	Basisisolierung (Schutzklasse 1, EN61140) basic insulation (class 1, IEC 61140)			Al_2O_3		
Kriechstrecke Creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			10,0 10,0		mm
Luftstrecke Clearance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			7,5 7,5		mm
Vergleichszahl der Kriechwegbildung Comperative tracking index		CTI		> 225		
			min.	typ.	max.	
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,009		K/W
Modulstreuinduktivität Stray inductance module		L_{sCE}		21		nH
Modulleitungswiderstand, Anschlüsse - Chip Module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		1,80		mΩ
Lagertemperatur Storage temperature		T_{stg}	-40		125	°C
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M5 - Montage gem. gültiger Applikationsschrift Screw M5 - Mounting according to valid application note	M	3,00	-	6,00	Nm
Gewicht Weight		G		300		g

Vorläufige Daten
Preliminary Data

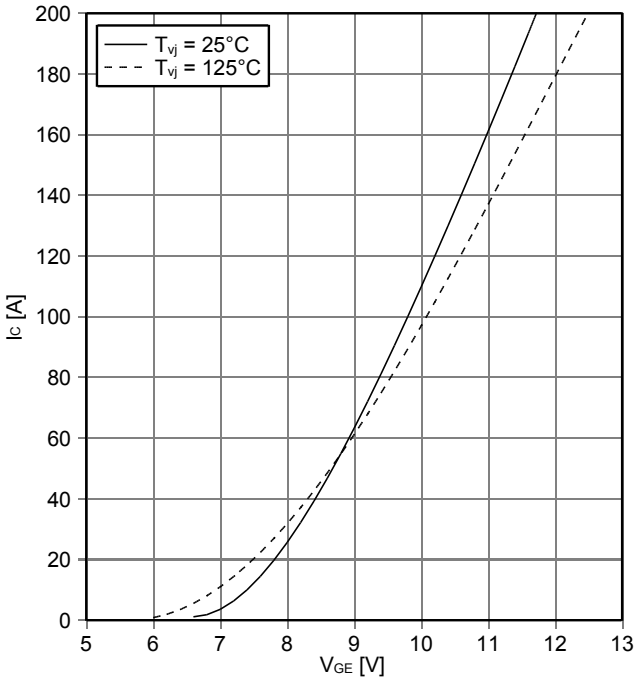
Ausgangskennlinie IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



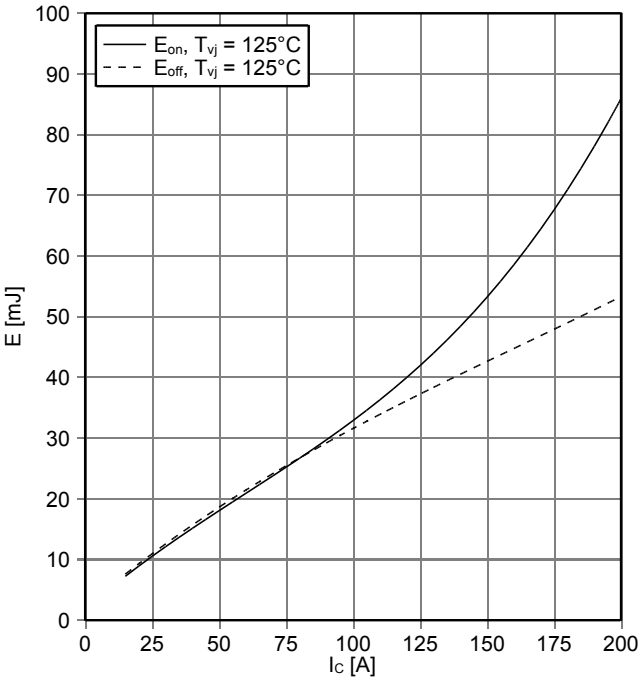
Ausgangskennlinienfeld IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 125°C



Übertragungscharakteristik IGBT,Wechselrichter (typisch)
transfer characteristic IGBT,Inverter(typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V



SchaltverlusteIGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 4 Ω, R_{Goff} = 4 Ω, V_{CE} = 900 V



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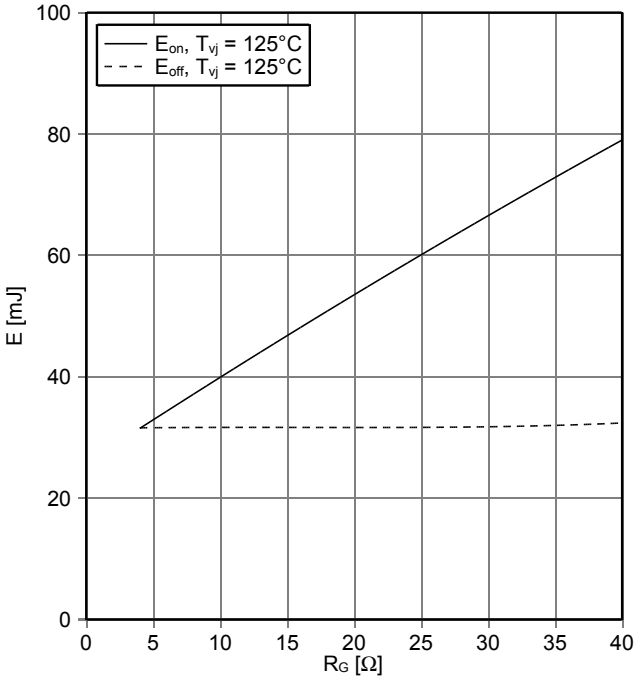
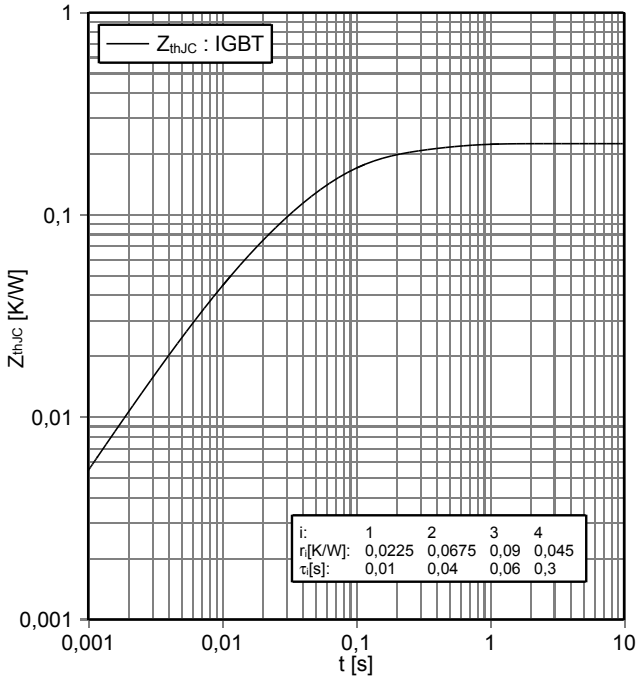
Vorläufige Daten
Preliminary Data

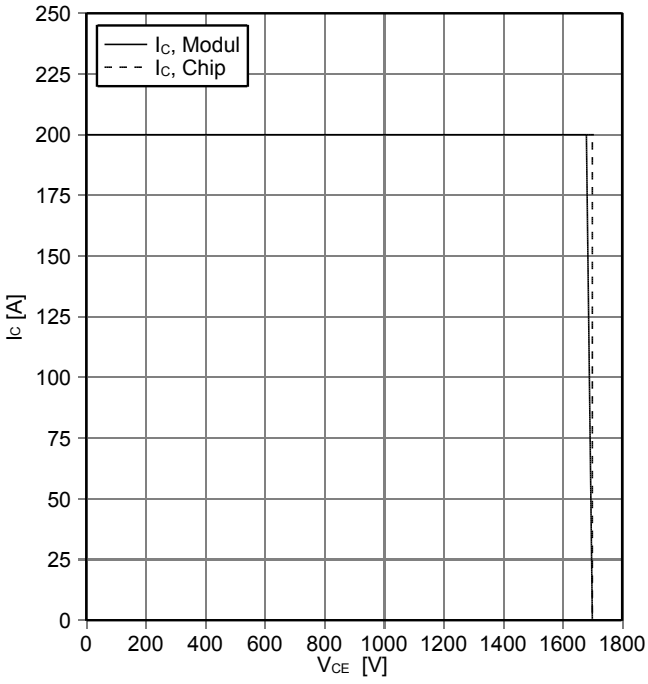
SchaltverlusteIGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GE} = ±15 V, I_C = 100 A, V_{CE} = 900 V



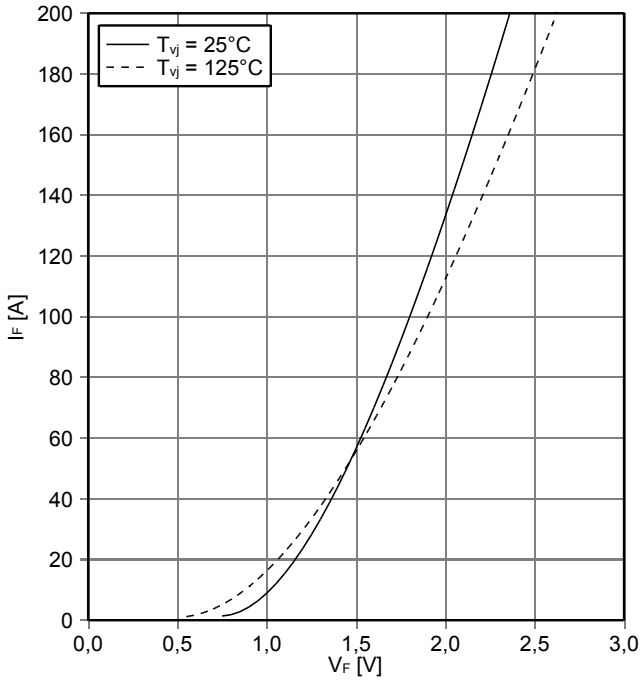
Transienter Wärmewiderstand IGBT,Wechselrichter
transient thermal impedance IGBT,Inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT,Wechselrichter (RBSOA)
reverse bias safe operating area IGBT,Inverter (RBSOA)
$I_C = f(V_{CE})$
V_{GE} = ±15 V, R_{Goff} = 4 Ω, T_{vj} = 125°C



Durchlasskennlinie der Diode, Wechselrichter (typisch)
forward characteristic of Diode, Inverter (typical)
$I_F = f(V_F)$



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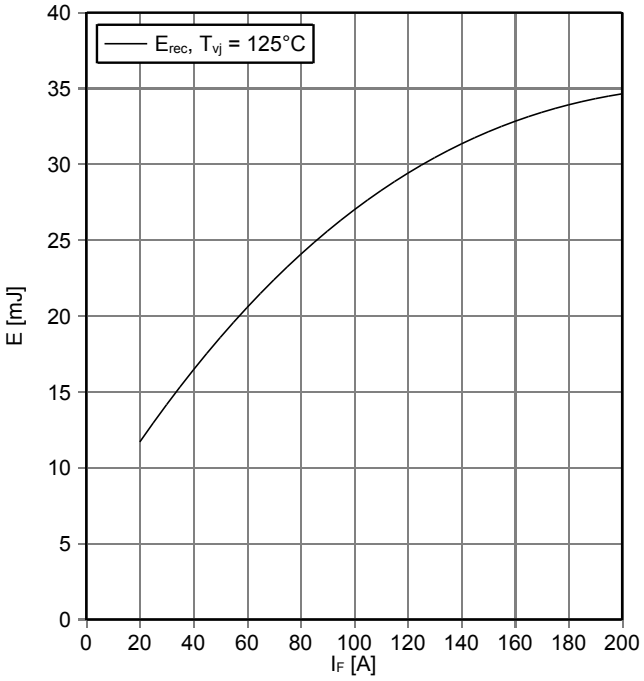
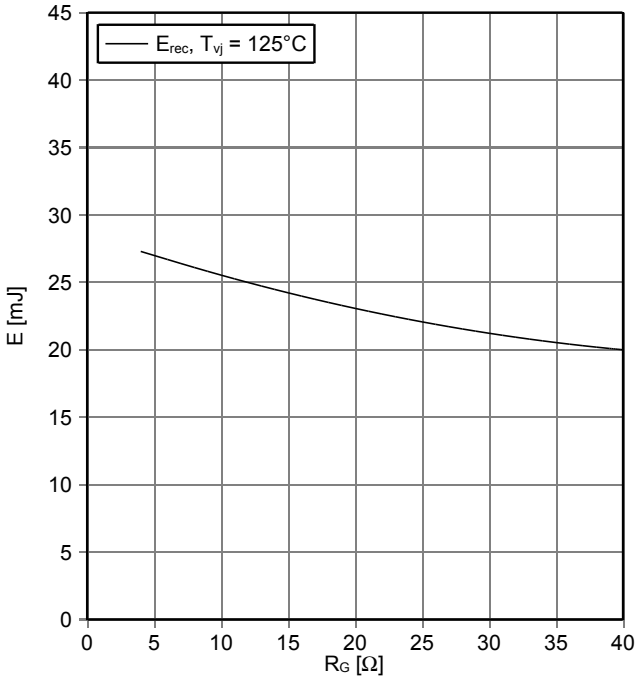
Vorläufige Daten
Preliminary Data

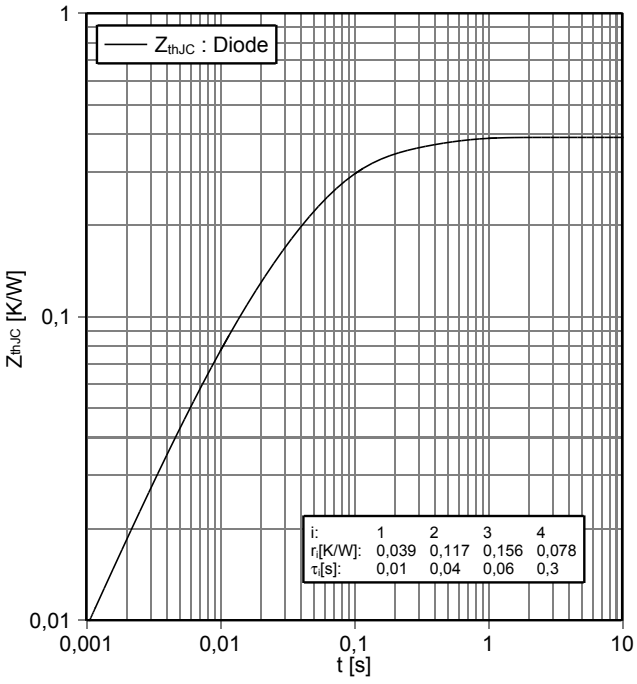
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 4\ \Omega$, $V_{CE} = 900$ V



Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 100$ A, $V_{CE} = 900$ V



Transienter Wärmewiderstand Diode, Wechselrichter
transient thermal impedance Diode, Inverter
$Z_{thJC} = f(t)$



prepared by: MW	date of publication: 2013-10-03
approved by: WR	revision: 2.0

Appendix B

Matlab script

The full implementation of the Matlab script file is shown below.

```
%clear;clc;close all;

%% Sizing
%*****************************

%------EDIT-->>>
V_DC = 350*3;
m_a = 0.9;
f_p = 50;
P_rated = 100E3;
Nc = 3;
% short circuit limits
P_sc = 0.01*P_rated;
Z_sc = 0.1;
%<<<------------
levels = Nc;
V_bat_unit = V_DC/levels;
V_ac = V_bat_unit*m_a*levels/sqrt(2);

% minimal sizing of the filter according to short circuit limits
R_t = P_sc*(V_ac/P_rated)^2;
Z_t = Z_sc*V_ac^2/(P_rated);
X_t = sqrt(Z_t^2-R_t^2);
L_t = X_t/(2*pi*f_p);

%% Time settings
```

```
%******************************

%time constants
%------EDIT-->>>
% time step of the solver
T_s = 0.00001;
% switching period
T_sw = 0.001;
% period of the grid fundamental
T_p = 1/f_p;
%<<<------------

% corresponding frequencies, inverse of the time constants
f_s = 1/T_s;
f_sw = 1/T_sw;
% moving average filter settings
FIR_MA_coeff = ones(1,round(1/f_p/T_s))/round(1/f_p/T_s);
MA_p = ones(1,round(1/f_p/T_s))/round(1/f_p/T_s);
MA_sw = ones(1,round(1/f_sw/T_s))/round(1/f_sw/T_s)

%% Control
%******************************

tau = T_sw/6;
T_n = L_t/R_t;
T_i = tau/R_t;

PID_P = T_n/T_i;
PID_I = 1/T_i;

%% Component parameters
%******************************
%  IGBT Module FS100R17KE3

% CONDUCTION LOSSES

%------EDIT-->>>
%diode (fit of exponential as voltage drop and linear resistance)
V_f = 1.083;
R_f = 7.638E-3;
%IGBT (fit of exponential as voltage drop and linear resistance)
V_ces = 0.923;
```

```
R_ce = 13.01E-3;
%<<<------------

% when turned off, the ideal diode and switch need to have a finite
   resistance
% the values are set in order to prevent pushing the diode unwanted in
% conduction mode
G1 = 1E-16;
G2 = G1/2*(V_bat_unit/V_f-1)*1.5;

% SWITCHING LOSSES

% points from datasheet graph
%------EDIT-->>>
% IGBT turn on points
I_on_vals = [25.35, 50.69, 76.04, 101.0, 126.4, 151.7, 176.7, 201.7];
E_on_vals = [10.77, 18.31, 25.69, 33.38, 42.62, 54, 68.46, 86.77]*1E-3;
V_ref_on = 900;
% IGBT turn off points
I_off_vals = [25.35, 50.69, 76.04, 101.0, 128.1, 151.7, 176.7, 199.3];
E_off_vals = [10.62, 18.92, 25.69, 32, 38.15, 43.23, 48.62, 53.54]*1E-3;
V_ref_off = 900;
% diode reverse recovery points
I_rec_vals = [20.35, 40.70, 61.05, 81.40, 102.1, 122.5, 142.5, 163.2, 183
   .9, 203.2];
E_rec_vals = [11.91, 16.73, 20.86, 24.44, 27.47, 29.94, 31.85, 33.40, 34
   .51, 35.19]*1E-3;
V_ref_rec = 900;
%<<<------------

% least-square polynomial fitting (order 2)
k_rec = polyfit(I_rec_vals,E_rec_vals,2);
k_on = polyfit(I_on_vals,E_on_vals,2);
k_off = polyfit(I_off_vals,E_off_vals,2);
a_rec = k_rec(1);b_rec = k_rec(2);c_rec = k_rec(3);
a_on = k_on(1);b_on = k_on(2);c_on = k_on(3);
a_off = k_off(1);b_off = k_off(2);c_off = k_off(3);
```

Appendix C

Simulink model

The Simulink model is a graphical description of the system. Fig. C.1 shows the highest level diagram. The Simulink tool allows the user to define new blocks, consisting of lower level blocks which generate outputs for given inputs. Fig. C.2 to C.6 show the implementation of important custom blocks. The model descriptions were slightly simplified for clarity, omitting scopes and other non-essential elements.

Finally, Fig. C.7 shows an augmented implementation of the block shown in C.3. This altered implementation automatically adapts the PWM when a battery module becomes unavailable. This implementation leads to the result shown in Fig. 5.12.

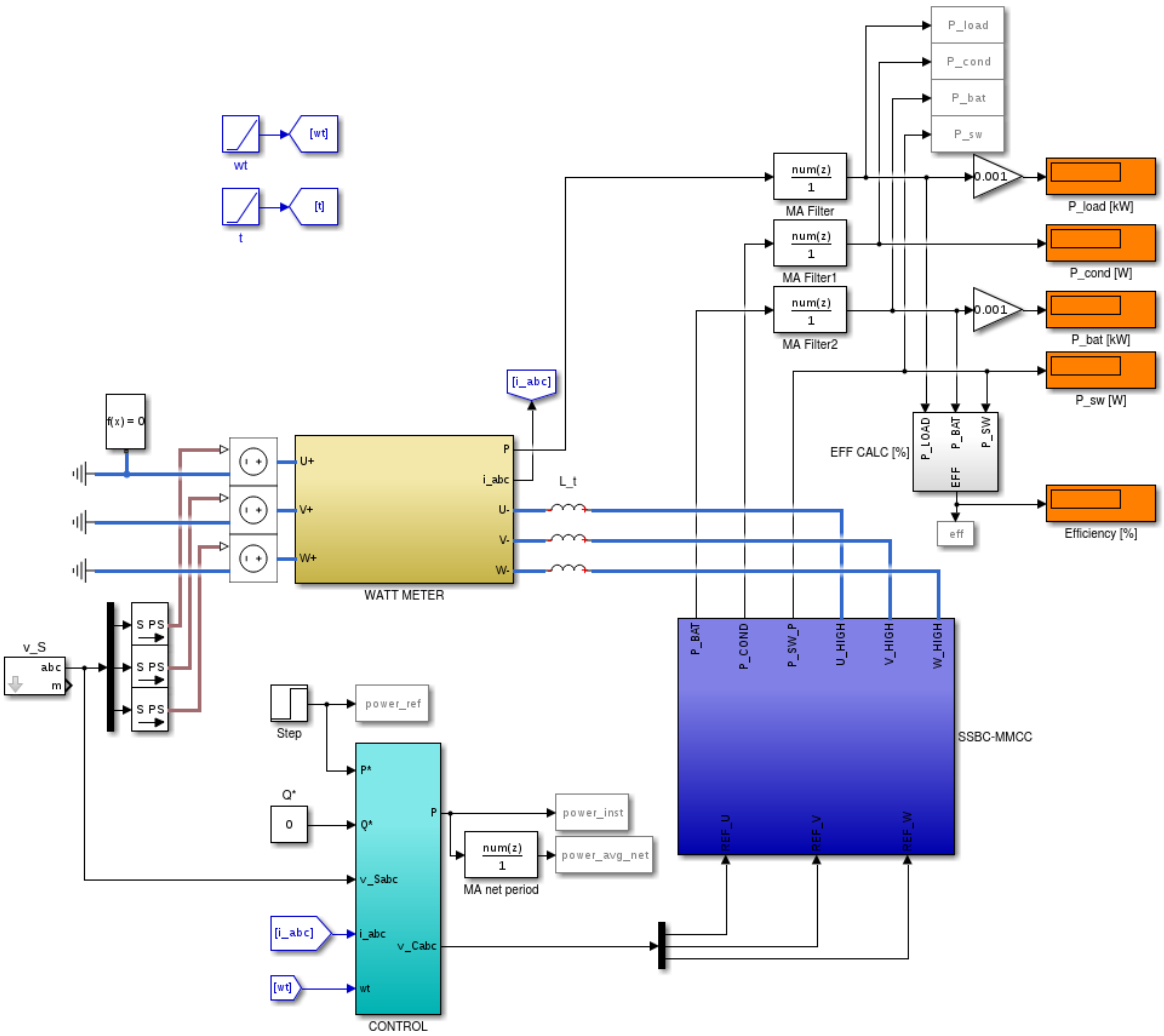
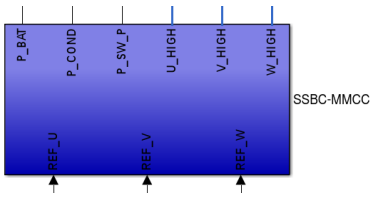
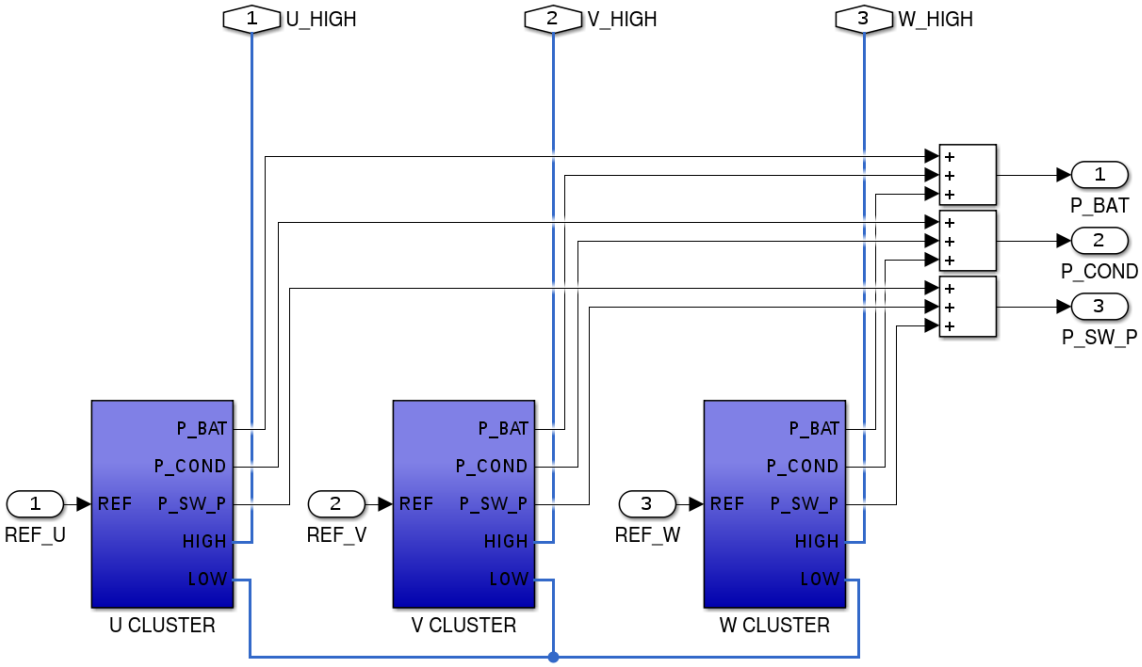


Figure C.1: The highest level diagram implements the top layer of the model: interface and control.

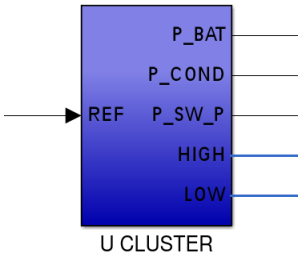


(a) Block symbol

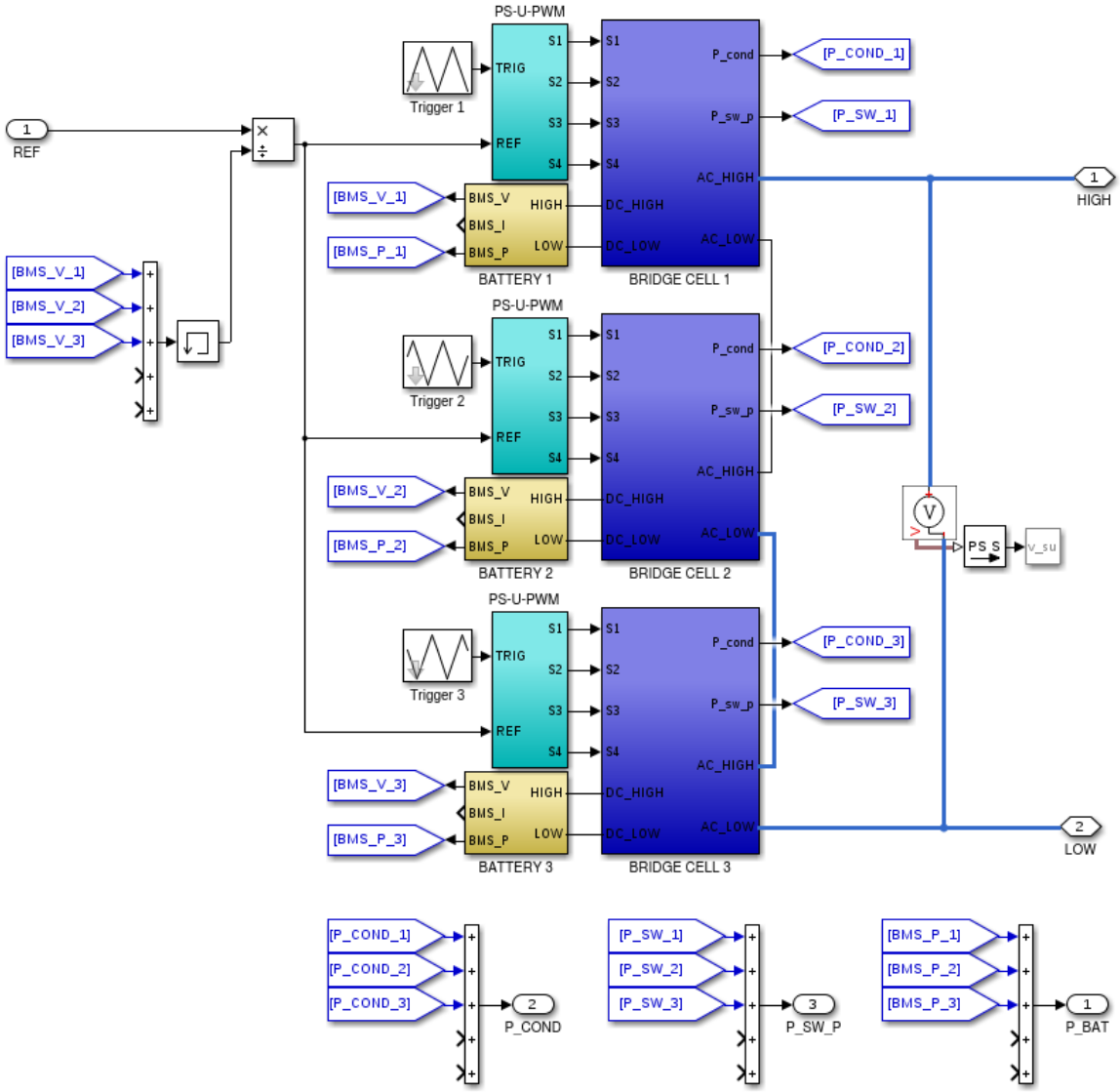


(b) Implementation

Figure C.2: The converter contains three clusters, one for each phase.

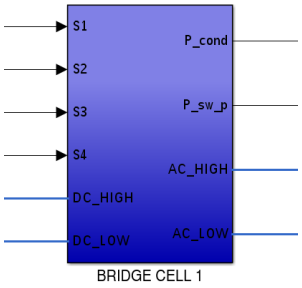


(a) Block symbol

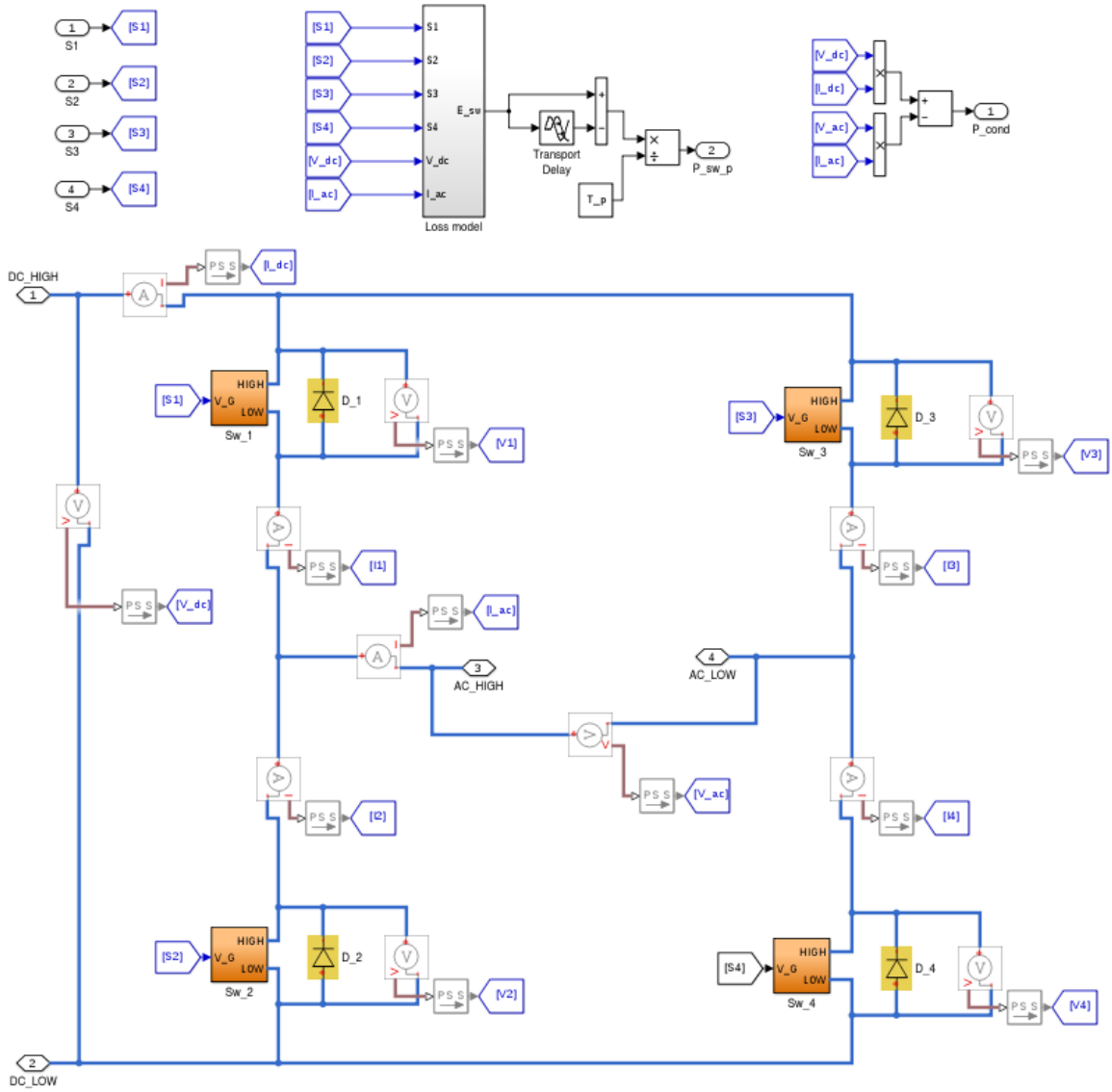


(b) Implementation

Figure C.3: This is an example of an implementation of a cluster containing three modules, $N_c = 3$. Increasing N_c simply means adding more modules in series, and changing the phase shift of the carriers. Changing the phase shift can be automated, shown by Fig. C.7.

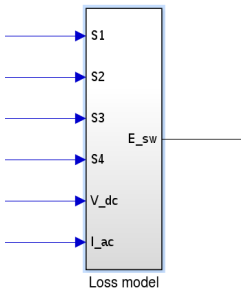


(a) Block symbol

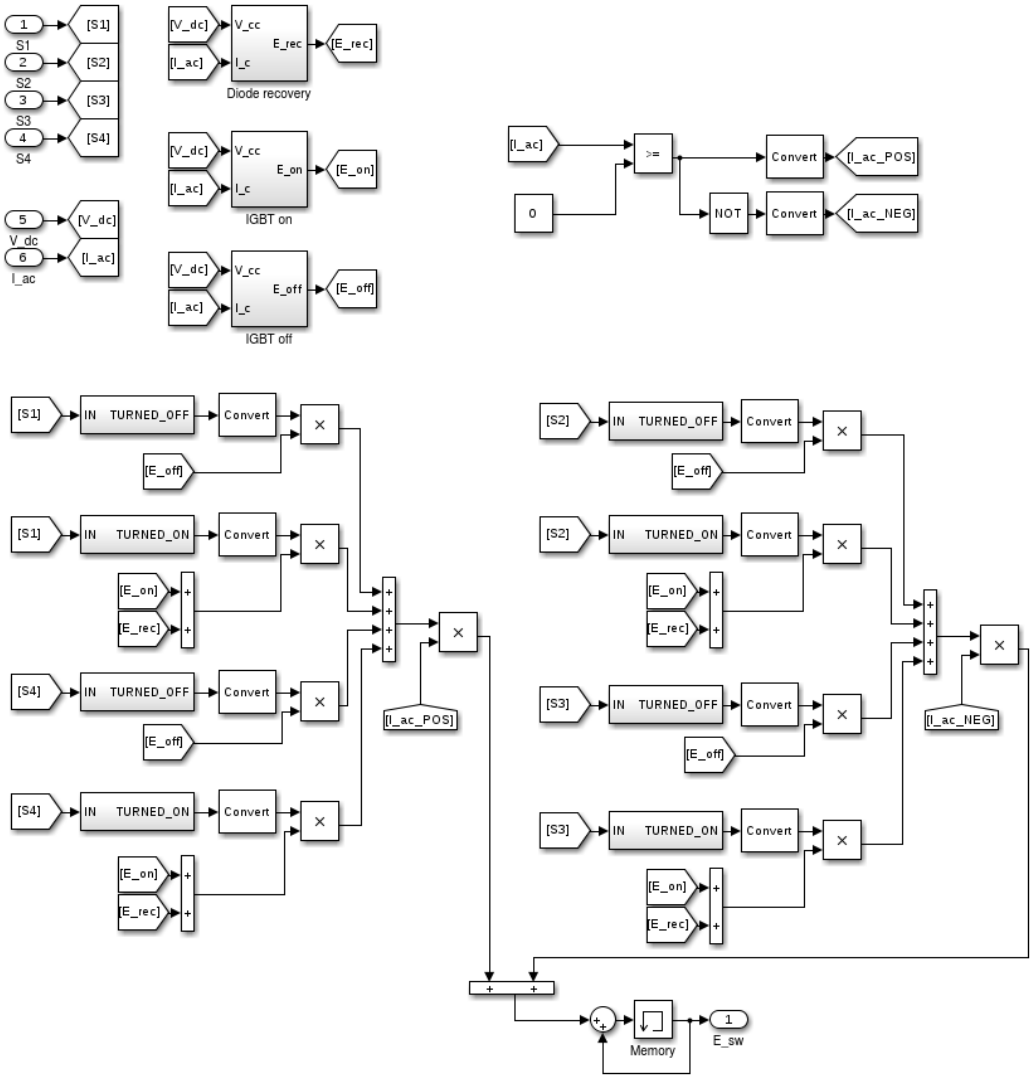


(b) Implementation

Figure C.4: An H-bridge contains 4 IGBTs and 4 diodes. The IGBTs are represented by a custom block, consisting of two anti-parallel ideal diodes in series with an ideal switch.

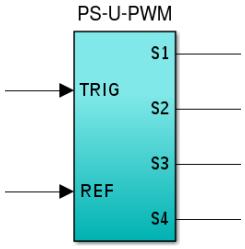


(a) Block symbol

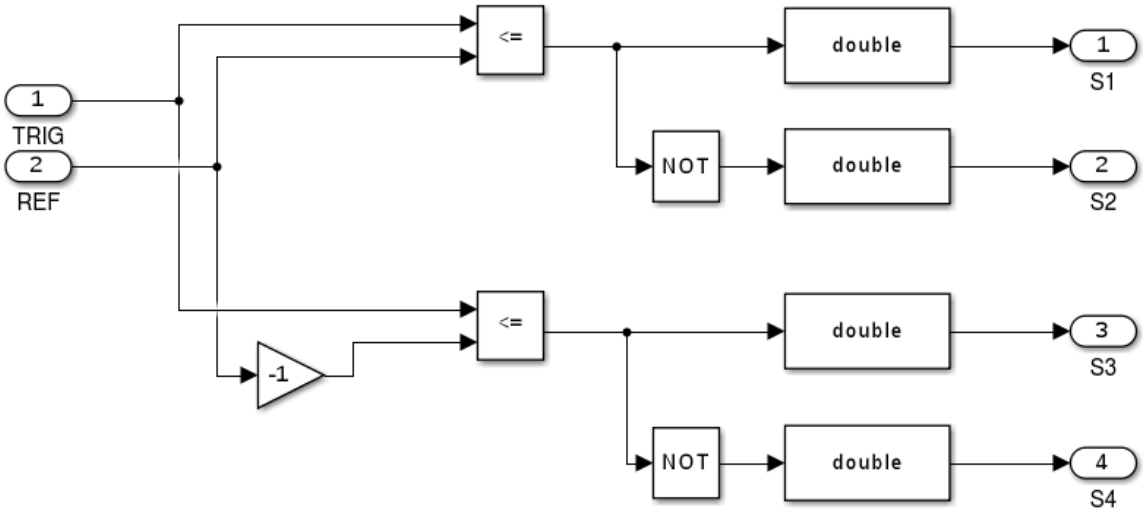


(b) Implementation

Figure C.5: The loss model monitors the switch state signals to look for switching events.

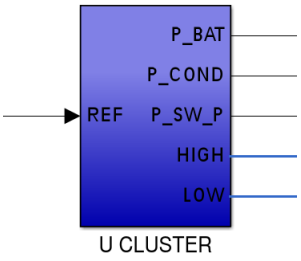


(a) Block symbol

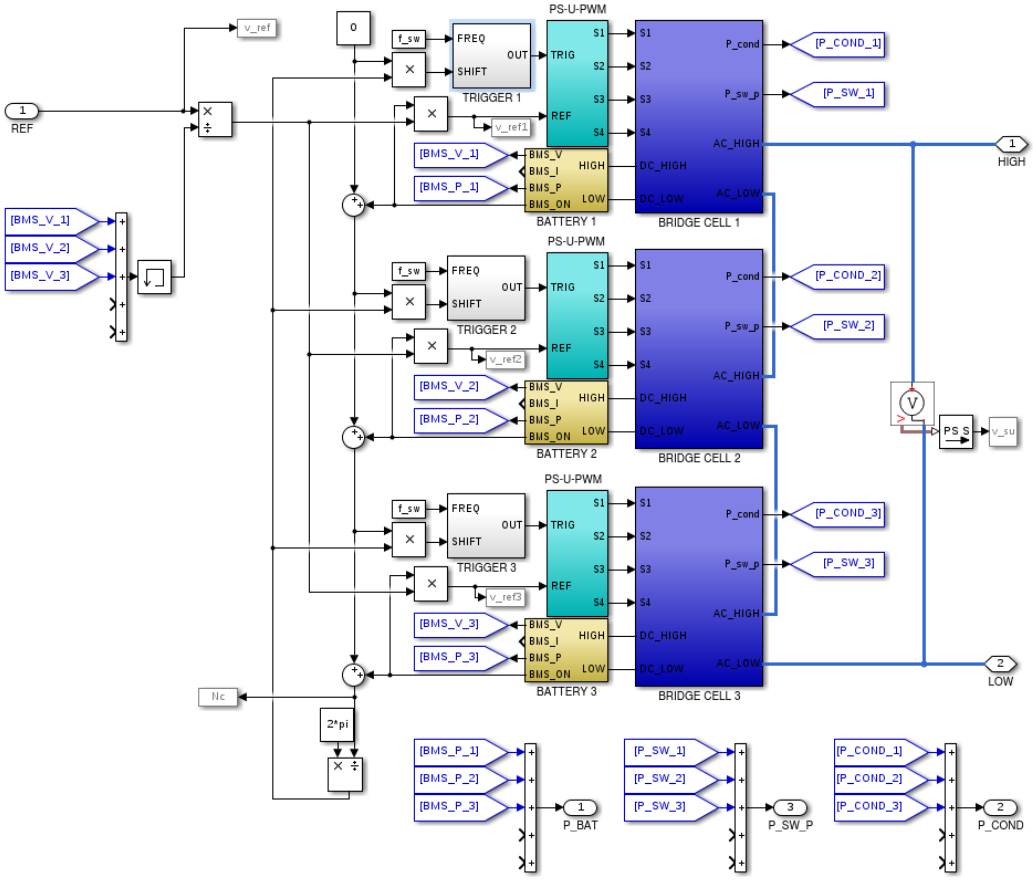


(b) Implementation

Figure C.6: The U-PWM block compares the trigger to the reference in order to generate the switch state signals.



(a) Block symbol



(b) Implementation

Figure C.7: This is an augmented version of the cluster implementation shown by Fig. C.3. Each battery module has a battery monitoring system (BMS), which indicates whether the battery is operational or not. There could be many reasons for the battery to become unavailable: a detected short-circuit, a manual interrupt... The phase shifts and reference signals are automatically adjusted according to the number of available batteries.

Appendix D

dq0 transform

This appendix shows the full derivation of the transformation of Equation (4.1) to the dq0 reference frame.

$$\mathbf{M}_{dq0}^{-1}\begin{bmatrix} v_{Cd} \\ v_{Cq} \\ v_{C0} \end{bmatrix} - \mathbf{M}_{dq0}^{-1}\begin{bmatrix} v_{Sd} \\ v_{Sq} \\ v_{S0} \end{bmatrix} = L_{ac}\frac{d}{dt}\left(\mathbf{M}_{dq0}^{-1}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}\right) + R\mathbf{M}_{dq0}^{-1}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}$$

$$\begin{aligned}
\Leftrightarrow \begin{bmatrix} v_{Cd} - v_{Sd} \\ v_{Cq} - v_{Sq} \\ v_{C0} - v_{S0} \end{bmatrix} &= \mathbf{M}_{dq0}L_{ac}\frac{d}{dt}\left(\mathbf{M}_{dq0}^{T}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}\right) + R\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \\
&= \left(L_{ac}\mathbf{M}_{dq0}\frac{d}{dt}\mathbf{M}_{dq0}^{T} + R\right)\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + L_{ac}\mathbf{M}_{dq0}\mathbf{M}_{dq0}^{T}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \\
&= \left(L_{ac}\mathbf{R}_{\gamma}(\omega t)\mathbf{M}_{\alpha\beta\gamma}\mathbf{M}_{\alpha\beta\gamma}^{T}\frac{d}{dt}\mathbf{R}_{\gamma}^{T}(\omega t) + R\right)\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + L_{ac}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \\
&= \left(L_{ac}\begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} + R\right)\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + L_{ac}\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}
\end{aligned}$$

The definition of the symbols and some properties are listed below.

$$\mathbf{M}_{\alpha\beta\gamma} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \qquad \mathbf{M}_{dq0}(t) = \begin{bmatrix} \cos\omega t & \sin\omega t & 0 \\ -\sin\omega t & \cos\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \mathbf{M}_{\alpha\beta\gamma}$$

$$\mathbf{M}_{dq0}^{-1} = \mathbf{M}_{dq0}^{T} \qquad \mathbf{M}_{dq0}^{T}\mathbf{M}_{dq0} = \mathbf{M}_{dq0}\mathbf{M}_{dq0}^{T} = \mathbf{I}$$
$$\mathbf{M}_{\alpha\beta\gamma}^{-1} = \mathbf{M}_{\alpha\beta\gamma}^{T} \qquad \mathbf{M}_{\alpha\beta\gamma}^{T}\mathbf{M}_{\alpha\beta\gamma} = \mathbf{M}_{\alpha\beta\gamma}\mathbf{M}_{\alpha\beta\gamma}^{T} = \mathbf{I}$$

The first derivative with respect to time is given by

$$\begin{aligned} \frac{d}{dt}\mathbf{M}_{dq0}(t) &= \frac{d}{dt}\mathbf{R}_{\gamma}(\omega t) \cdot \mathbf{M}_{\alpha\beta\gamma} \\ &= \begin{bmatrix} -\omega\sin\omega t & \omega\cos\omega t & 0 \\ -\omega\cos\omega t & -\omega\sin\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \mathbf{M}_{\alpha\beta\gamma} \\ \frac{d}{dt}\mathbf{M}_{dq0}^{T}(t) &= \mathbf{M}_{\alpha\beta\gamma}^{T} \cdot \frac{d}{dt}\mathbf{R}_{\gamma}^{T}(\omega t) \\ &= \mathbf{M}_{\alpha\beta\gamma}^{T} \cdot \begin{bmatrix} -\omega\sin\omega t & -\omega\cos\omega t & 0 \\ \omega\cos\omega t & -\omega\sin\omega t & 0 \\ 0 & 0 & 1 \end{bmatrix} \end{aligned}$$